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KDF 9 - TRANSFORMER SEQUENCE UNITS

C.2.

Report by

J.R. Lucking.

SUMMARY

There are 8 transformer sequence units in the basic KDF 9 and this report describes the general principles of any such sequence unit. It introduces the terminology which will be used in future reports describing the individual sequence units in more detail.

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- 2.0. INPUT-OUTPUT SEQUENCE UNITS
- 3.0. MAIN CONTROL AND ARITHMETIC CONTROL SEQUENCE UNITS

APPENDIX I The Paper-tape Punch Buffer

1. GENERAL

In KDF 9, a machine instruction is performed by a sequence of 'micro-instructions' (MI's), each micro-instruction being a combination of pulse excited basic actions. These basic actions may be transfers between registers or indicators, transfers of logical conditions to registers or indicators, setting of registers or indicators to predetermined states or the initiation of some other independently controlled sequence unit. Examples of basic actions are:-

- (i) Transfer contents of the register NB to the register W3 (See Arithmetic Unit);
- (ii) Set sum of contents of registers A and QM into register B (See Q-mill);
- (iii) Read contents of the Q-store whose address is in QSAR into the register QB;
- (iv) Start a main store cycle - note there is an elementary sequence unit in the main store cubicle.

Nearly all of these basic actions are effected by exciting a suitable pulse amplifier.

Most of the actions are common to several different micro-instructions and some are common to different sequence units. The actions, the micro-instructions and the sequences of micro-instructions are all 'wired-in' features of the KDF 9.

1.1 Micro-instructions and Sequence Units

A micro-instruction is performed by pulsing a transformer whose output windings are connected to the pulse amplifiers which control the desired basic actions; these output windings may be gated by some d.c. level generated outside the sequence unit to provide conditional MI's. Thus the MI - 'IF QM is positive THEN clear QC and QI' may be obtained by gating, with a d.c. level controlled by the sign digit of QM, the output winding connected to the pulse amplifiers clearing QC and QI.

A transformer used this way is called a sequence unit transformer (SUT). Besides the output winding just described, and SUT carries other secondary windings (selection windings) which specify the SUT to be pulsed next. These selection windings modify (this modification may be conditional as for MI's) the contents of a register which controls decoding circuitry for selecting one of a number of SUT'S. This register is called a 'micro-instruction staticisor' (MIS) and the binary pattern it contains a 'micro-instruction code' (MIC): thus every SUT has a unique MIC. Obviously the MIS selecting the current SUT cannot be allowed to change while that SUT is pulsed, so a sequence unit

employs two MIS registers which are used alternately. For this, and other engineering reasons, the SUT's are also divided into two groups - one to each MIS. Such a group of SUT's is occasionally called a sequence unit matrix (due to selection techniques used).

Figure 1 illustrates the principles outlined above.

1.2 Selection techniques based on the MIS.

This section describes the logic attached to an MIS register which selects the SUT whose MIC is contained in that MIS. In the larger sequence units, for economy of logical elements, this selection is normally divided into two sections - the TOP selection (TS) and the BOTTOM selection (BS).

Top Selection

The 'n' most significant bits of the MIS are decoded into 2^n mutually exclusive d.c. levels, each of these levels gates a transformer secondary supplying a pulse amplifier. Thus for any MIC, only one of the 2^n amplifiers is operated when the transformer is pulsed (by a clock pulse). The input, or top end, of the SUT primaries are connected to the appropriate pulse amplifiers.

Bottom Selection

The remaining (least significant) bits of the MIS register are decoded into d.c. levels operating d.c. gates which are connected to the gating (or bottom) ends of the appropriate SUT primaries.

Figure 2 shows the selection for a 4-bit MIC and explains the use of the term matrix for such a group of SUT's. The method is an example of the generation of 'AND' logic using transformers - thus a certain SUT will be pulsed if the top n bits of its MIC correspond to the top n bits in MIS and the bottom bits of its MIC correspond to those in the MIS.

The AC and MC sequence units use 6 bit MIC's; 3 bits are used for each of top and bottom selection (for this reason the codes are written in octal). Many of the smaller sequence units in input-output equipment use only 4 bit codes and do not employ top selection (e.g. the sequence unit in the paper tape reader buffer).

1.3 Use of the Selection Windings: Sequencing.

Each SUT must specify the code of its successor (see 1.1), i.e. cause this MIC to be set up in the MIS next to be used. This is done by the selection windings; two different techniques are used:

- i) Modification of the previous contents of the MIS. This is done by changing only one or two digits

of the MIC and is used in the simpler sequence units.

- ii) Complete replacement of the MIS. This is used in both MC and AC, and requires 6 selection windings (one for each bit of the MIC) on each SUT.

The succeeding MI required depends on the micro-program being executed, and also, in many cases, on some logical condition. By using suitable d.c. levels to gate the selection windings, one of a number of MIC's is set up. Two classes of gating condition are used:-

- i) Function levels - i.e. the sequence unit is generating the micro-program for a specific instruction (e.g. peripheral write). This function level will gate most SUT's used in the sequence.
- ii) Conditional branching levels (or masks). This selects one of two possible branches in a micro-program, depending on some logical condition e.g. a test by MC to see if the main store is free; if not, MC must wait (executing a small loop of 2 MI's) until the store is free, at which time it continues the 'normal' micro-program. These levels correspond to conditional transfers of control in programming language.

1.4 Allocation of Codes to Micro-instructions.

This paragraph demonstrates by means of an example how the selection windings are used to select the next micro-instruction and what limitations are placed on the codes allocated to micro-instructions. Suppose that a micro-instruction MI_x, which is used in several sequences, is used in the sequence Sz, and will specify one of two micro-instructions MI true and MI false dependent on a logical condition called 'alpha'. Thus MI_x may be written.

MI_x: Perform various basic actions;

If function level Sz is present and 'alpha' is true then set code 'MI-true' in MIS;

If function level Sz is present and 'alpha' is false then set code 'MI-false' in MIS.

Then the setting of the code into MIS is normally performed using two separate selection windings. The first winding (or group of windings) is connected to the function level Sz, and sets the code of 'MI false' into MIS (by direct setting of ones in AC/MC; or by changing only the necessary digits of the previous contents of MIS in IOC). The second winding (or group of windings) is gated by the logical level 'alpha', and by operating only on those digits of the MIS not affected by the setting of 'MI false' changes the code (from that of 'MI false') into the code of 'MI true'. This is achieved either

- i) by setting one/s where zero/es existed in 'MI false', (in AC/MC) or
- ii) in IO by changing (either to zero or one) some digit of the previous contents of MIS which is not affected by setting 'MI false'.

i.e. In AC/MC.

Let MI false be 011001

MI true be 011011

Then the presence of 'Sz' causes digits 1, 2 and 5 to be set. (the absence of setting pulse to digits 0, 3 & 4 causes them to be cleared - see later).

The presence of 'alpha' causes digit 4 to be set, converting 'MI false' Code to the 'MI true' Code.

In IOC.

Let MI false = 0110

MI true = (a) 1110
(b) 0010

The previous contents of MIS were

0111

Then presence of 'Sz' causes d_3 to be cleared;
and the presence of 'alpha' causes

- a) d_0 to be set,
- or b) d_1 to be cleared.

The important restrictions on codes, shown in the above example may be summarised:-

- i) When following a branch, both the function level and the conditional branching level will be present simultaneously, thus
- ii) The MIC bits set up by the function level must be the same for the 'normal' path and the branch,
- iii) it follows that the branching level must only set up bits not affected by (ii).

2. INPUT-OUTPUT SEQUENCE UNITS

2.0. General

Input/Output Control contains 3 sequence units:-

- i) RSU: Sets up and clears down peripheral instructions and controls the lockout circuits
- ii) ESU1) Supervise the transfer of data
- and iii) ESU2) between the Buffer units and Main store
- iv) In addition each buffer contains a sequence unit.

These sequence units vary in size, the smallest having only two groups of 8 SUT's, and the largest two groups of about 33 SUT's.

Standard 3-secondary transformer packages (K293/10) are used to provide the SUT's; if more than 3 secondaries are required, two (or more) of the standard transformers are used (with their primaries connected in parallel). An engineering limitation of transformers in parallel (18 secondaries) is applied. The secondaries (+3.3v output) may be used either as output or selection windings; and can be gated at the standard logical levels

i.e. Logical 1 is 0 to $-\frac{1}{3}$ V.

The next MIC is set up by changing only those bits necessary in the MIS (normally only one bit is changed). This leads to a considerable economy in selection windings.

IO sequence units do not employ function levels in the same sense as do those of AC and MC. Rather, they employ a 'fixed' micro-program, with (in the case of the more complex units e.g. RSU) a number of branches (and loops). The majority of micro-instructions available are unique to a particular branch, (i.e. are not used elsewhere in the micro-program,) and so a particular branch, once entered by the presence of the appropriate conditional branching level, is followed through without having to apply 'same common function level' to all the SUT's used. In such sequence units a branch will often correspond to the bulk of the micro-program required to complete (in that sequence unit) a machine instruction.

e.g. The setting up of a peripheral read (or write) is a major branch in the RSU.

2.1 Allocations of Micro-Instruction Codes.

The general principles employed are best illustrated with a specific example. Appendix 1 describes fully the sequence unit employed in the paper tape punch buffer: this is one of the simplest units used.

3. MAIN CONTROL AND ARITHMETIC SEQUENCE UNITS

These sequence units are very similar. Both use:-

- (i) Two groups of 64 SUT's
- (ii) for each group a 6 bit MIC with 3 bit Top Selection and 3 bit Bottom Selection.
- (iii) Special SUT packages.
- (iv) Each SUT carries 6 selection windings, so that the contents of MIS are completely replaced when a SUT is pulsed.
- (v) Two sets of 6 'complementing' amplifiers.

The outputs of the equivalent selection windings on all SUT's are connected in parallel to one of these amplifiers, which is also supplied with the pulse driving the SUT. If there is no output from the selection winding this amplifier clears the corresponding bit of MIS, if there is an output the bit is set to one. Note that if these complementing amplifiers were not used then every SUT would have to carry 12 selection windings, and 'masking' (see below) would be more complex.

3.1 Special SUT packages for MC & AC

Special boards of SUT's are used in AC and MC; these boards contain respectively 2 and 4 SUT's whose selection winding outputs have been joined. Diodes may be inserted in standard positions on these boards, to form 'OR' gates of function levels and branching conditions onto the selection windings. Fig. 3 illustrates this principle. The SUT boards provide:-

Board No. K552A

No. of SUT's carried = 2
No. of function (or masks) lines = 12
Each of these levels may be 'ORed' onto all the selection windings of the two SUT's.

The primaries, and the 2 output windings of both SUT's are completely independent

Board K551A

No. of SUT's carried = 4 named A, B, C and D.
No. of function lines = 8 numbered 0-7.
4 lines, 0-3 may be 'ORed' onto the selection windings of SUT A

8 lines, 0-7 may be 'ORed' onto the selection of windings of SUT B.

4 lines, 4 - 7 may be 'ORed' onto the selection of windings of SUT C

6 lines, 2 - 7 may be 'ORed' onto the selection of windings of SUT D.

Primaries: Common top selection.

Output Windings: 2 per SUT, only one of these

windings is completely independent - the other winding has a common return path for all 4 SUT's.

The primaries and output windings of these SUT's use the standard ratio's (-10V pulse drive and a + 3.3 V output) the selection windings are designed to operate from gates with a logical ONE output of -2.0V to -2.5V as opposed to the standard earth 'ONE' level (0 to - 0.5V). These d.c. gates impose a lighter load on their inputs (normally the AC or MC instruction staticiser registers), and also allow a better discrimination against noise pulses picked up in the selection winding wiring.

The use of these special boards has simplified the problem of allocating codes to MI's and leads to economy of space and wiring in the MC and AC sequence units. For a few MI's additional output windings are required and in these cases a standard transfer transformer is connected in parallel with the SUT.

3.2 Masking and Function Levels

This section details those restraints which must be applied to M.I. codes so that correct sequencing will result. These require that proper notice be taken of:-

- (i) the function level, i.e. what instruction is being obeyed, and
 - (ii) any logical levels, indicating the state of the machine which may modify or prevent the execution of this instruction - thus MC may not use the main store if IOC is using it.
- (a) Function Levels These are provided by a set of - 2V d.c. gates no two of which are ever simultaneously switched on. These levels must be connected to the selection windings of all SUT's used in the (microprogram) sequence for obeying the corresponding instruction/s.
- (b) Conditional Branching (Or Masking) levels Again these are provided by a set of -2V d.c. gates, driven by the indicators, or conditions these levels represent, and are connected to the selection windings of the relevant SUT's. They have been termed 'masks' as their only function is to overwrite 'ones' into selected digit positions of the MIS defining the next MIC. The use of these levels is best shown by examples:-

- (i) A simple branch

MI .1 Actions:- transfer register QM to register A.

Function:- Direct store instruction(MC).

Mask:- Is SBAR full ?



A possible set of codes is:-

MI.2 = 0 1 1 0 0 1 (= 3,1 in octal)

MI.3 = 1 1 1 0 0 1 (= 7,1 in octal)

Diodes are inserted in positions to connect this function level to selection windings number 1,2,5 of the SUT corresponding to MI1. The masking condition, which indicates that there is an outstanding store instruction to be performed, is connected to winding 0. Thus:-

Function level above sets 0 1 1 0 0 1
Masking condition sets 1(0 0 0 0 0)

(ii) A 4-way branch -- (this example is hypothetical).

MI 1 -- Actions:-

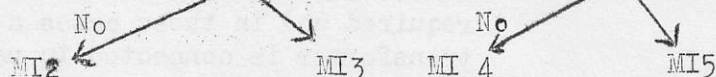
Functions:-

Masks:- Is indicator x set?

No.

Is indicator y set?

Is indicator y set?



a possible set of codes is:-

MI2	0 0 0 1 0 0
MI3	0 0 0 1 1 0
MI4	0 0 0 1 0 1
MI5	0 0 0 1 1 1

Thus the function level above sets
0 0 0 1 0 0.

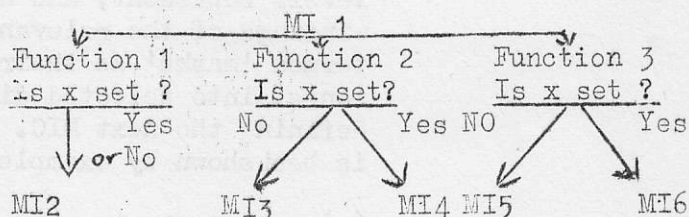
Mask corresponding to x indicator sets
0 0 0 0 0 1

Mask corresponding to y indicator sets
0 0 0 0 1 0

As may be seen, the only restrictions that this use of masks leads to is that the code of the micro-instruction, on the NO side of the branch must be 'included' in the code of the micro-instruction on the YES side.

More stringent conditions arise when a MI with a masking condition is used in different sequences and specifies different next MI's

(iii)



a possible set of codes is

MI2	1 0 1 0 0 1
MI3	0 0 0 0 1 1
MI4	1 0 0 0 1 1
MI5	0 0 1 1 0 0
MI6	1 0 1 1 0 1

Thus function 1 sets 1 0 1 0 0 1

2 0 0 0 0 1 1

3 0 0 1 1 0 0

Mask x sets 1 0 0 0 0 1

and the set of conditions is:-

Mask x contained in MIC 2.

MIC 3 plus (Logical 'or') Mask x = MIC 4

MIC 5 plus Mask x == MIC 6

In the main control sequence units, where there are a large number of multi-branch sequences, the restrictions which these conditions place on the codes allocated to the micro-instructions are fairly severe.

3.3. Saving of Equipment

Besides the restraints placed on MI codes to ensure correct sequencing, other restraints can be applied which simply save equipment and wiring. This can be illustrated by means of examples.

- (i) A micro-instruction is used in only one sequence or alternatively is used in more than one sequence but always specifies the same next micro-instruction. In these cases it is not necessary to supply any function levels to the SUT - instead the -2V bus is connected to the selection windings, to set the the required next MIC.
- (ii) A micro-instruction is used in several sequences and specifies different next micro-instructions whose codes have some bits in common. e.g. suppose MI1 is used

In sequence A and specifies MI2 next.

In sequence B and specifies MI3 next

In sequence C and specifies MI4 next.

and the codes for these micro-instructions are:-

0 1 1 0 0 0

0 1 1 1 0 1

1 1 1 0 0 0

then function level A need not be connected to the SUT (and can be replaced by the -2Vbus). This will generate the code 011000 every time this micro-instruction is pulsed. Thus function levels B and C merely generate the patterns 000101 and 100000. This saves diodes on the SUT boards and lightens the loads on the -2V dc gates.

- (iii) A micro-instruction is used in several sequences and specifies several different 'next' micro-instructions but groups of these sequences specify the same next MI. For example Micro-instruction I specifies the following next MI's.

MI2 in sequences ACDH

MI3 in sequences BGJKM

MI4 in sequence E

MI5 in sequence FIL.

This would require the 13 different function levels to be 'ORed' onto the SUT using the OR gates provided on the SUT boards. This number of function levels cannot be provided on one SUT package. Rather than use two SUT's (on separate boards but connected in parallel) to provide this step, the various combinations ACDH, BGJKN, FIL are ORed together outside the SUT board (using simple diode 'OR' gates) and then connected to the selection windings via the diode OR gates on the SUT board. This device shows little saving unless the combinations so generated are used on more than one MIC code; this may be ensured by introducing some redundancy, thus the combination ACDH may be used to produce the combination ADH on another micro-instruction (provided of course that this is not used in sequence C).

These last two techniques, i.e. using the -2V bus instead of a function level and producing combinations of functions, may of course be combined and in suitable circumstances save a considerable amount of equipment.

Such techniques were adopted in main control. They lead to further restrictions in the allocation of codes to MIC's, in order to produce the maximum saving. They introduce a number of complications; in particular they make it impossible to avoid a complete reallocation of codes (with the consequent rescheduling of the control unit) should it ever be required to make any but the simplest changes to the micro-programs. Also, the effect of these techniques must be considered when tracing any faults in such sequence units, as they allow some SUT's to generate a next MIC in the absence of a relevant function level.

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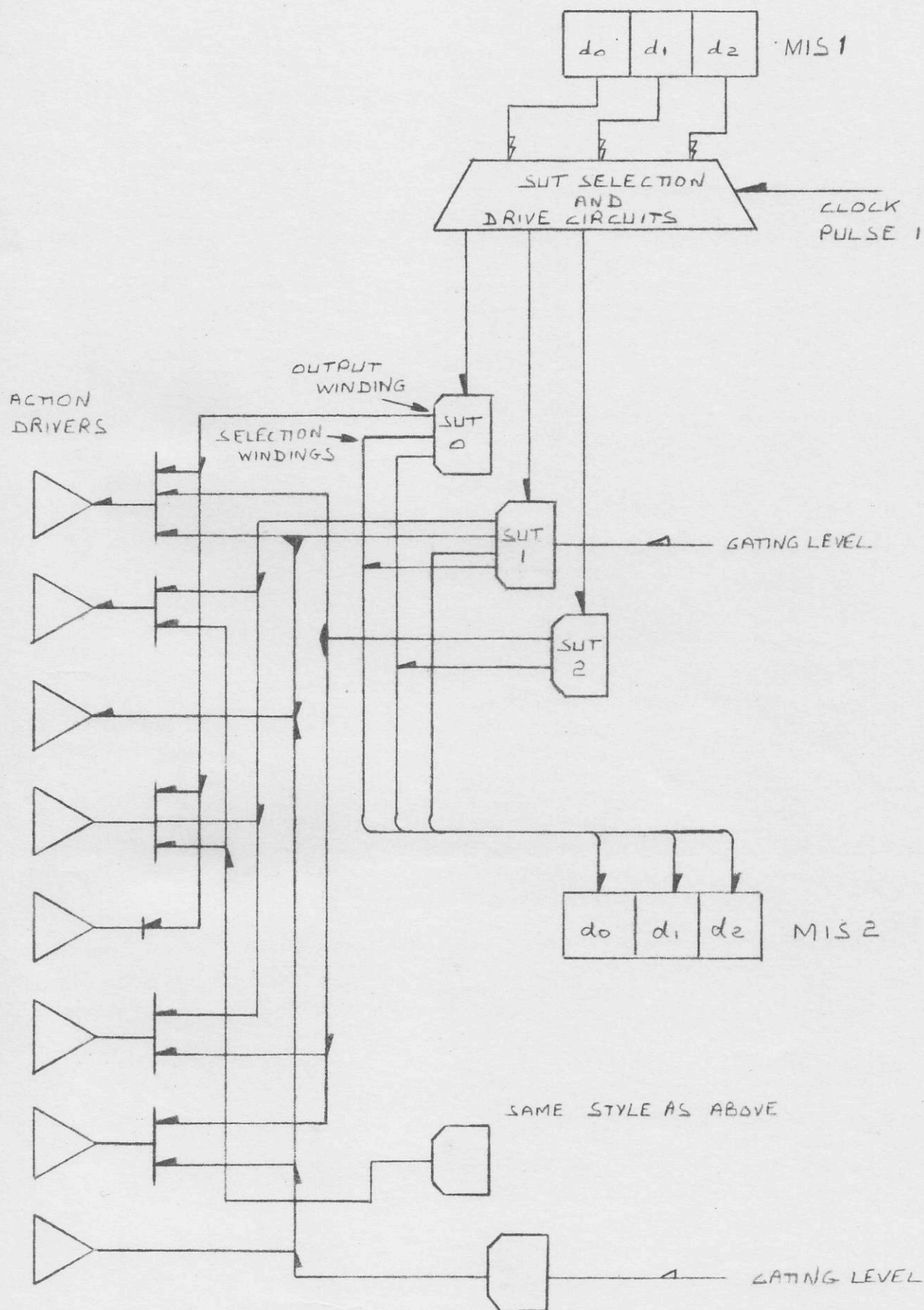
Chief Development Engineer
DP&CSD.

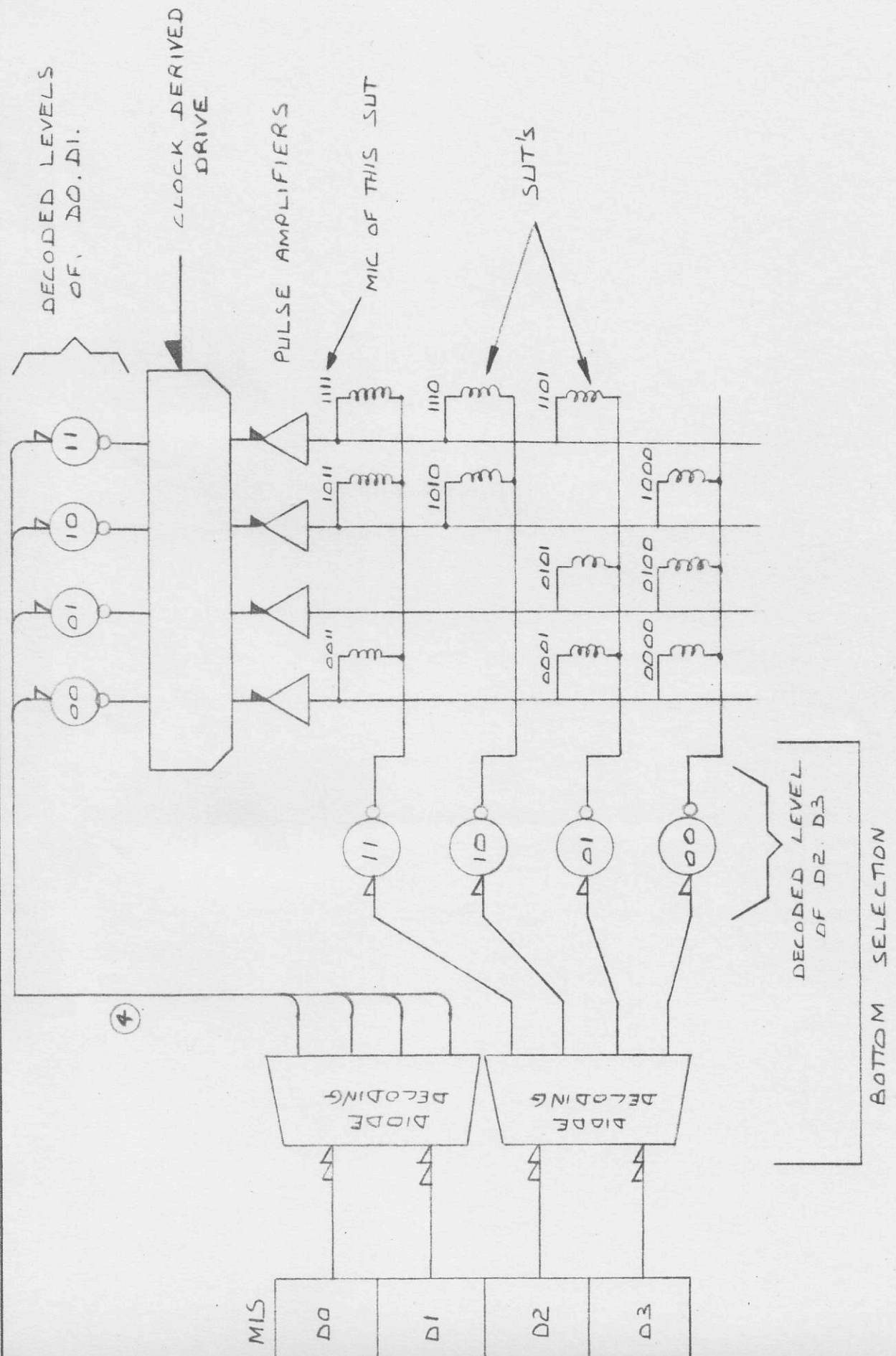
J.R. Lucking
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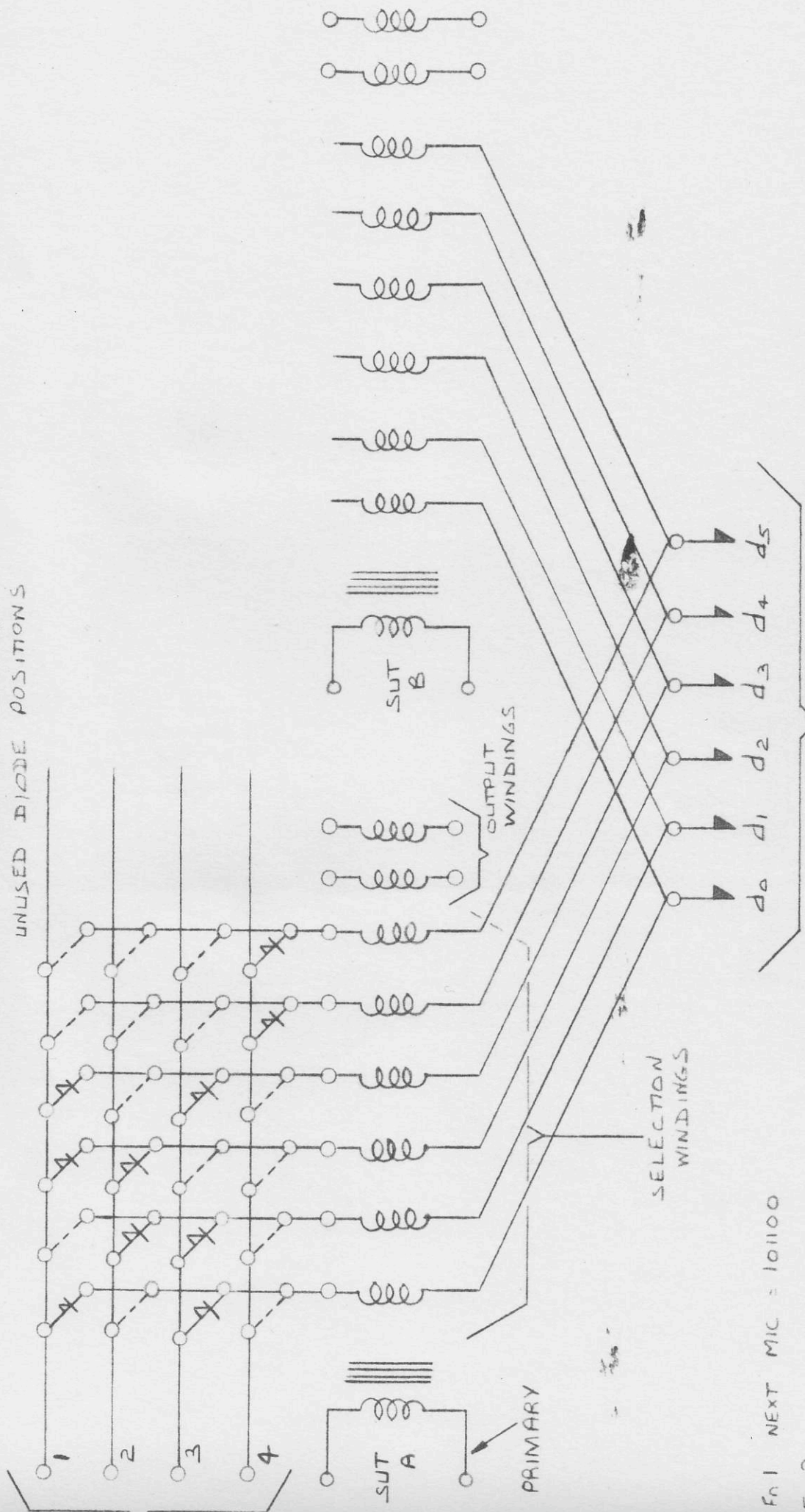
Enclosures: Figure Sheets. 1-3.

A TYPICAL SEQUENCE UNIT



SELECTION OF SUT'S

DOTTED LINES INDICATE
UNUSED DIODE POSITIONS



TO COMPLEMENTING AMPLIFIERS

F_n 1 NEXT MIC = 101100
F_n 2 " " 011000
F_n 3 " " 110100

APPENDIX IBRIEF DESCRIPTION OF THE PAPER-TAPE PUNCH BUFFER

This buffer, which occupies bin 2E in the BUFFER 1 cubicle, controls the operation of the paper-tape punch. The sequence unit controlling the buffer contains 2 banks of 5 SUTS controlled by two 3-bit registers - the LMIS and the UMIS. The SUT's are pulsed by two interlacing sets of P_i pulses, each bank of SUT's, being pulsed once every 4 microsec. The purpose of the buffer is to time the action of the solenoids in the punch which drive the punch knives once every cycle. Apart from the sequence unit itself, the punch buffer contains the following facilities.

- (i) An 8-bit register - the Character Buffer (CHB)
This register is filled by the ESU on receipt of a request from the Punch Buffer. It controls the energising of the 8 solenoids in the punch.
- (ii) One indicator END - this is set by the ESU when the last character to be punched is placed in the CHB.
- (iii) Two unready indicators - UR1, UR 2
UR1 is set by the RSU if the unready bit(INS(15)) in the peripheral transfer to be obeyed is set.
UR2 is set as soon as there is less than approx 10 feet of paper tape left on the reel. Thus blocks transfers of more than(approx.) 1000 characters to the paper tape punch should not be sttimmed.
Both these indicators are reset by operating the TAPE LO/ switch on the punch - this is performed when reloading.
- (iv) A Broken-tape indicator - BR
- (v) Three 'mode' indicators - WR, ERASE, and RET.
WR is set by RSU if the function to be obeyed is a write.
ERASE is set by RSU if the function to be obeyed is an "erase". Note that WR is also set as an erase is a Write instruction.
If Erase is set the 8 solenoids in the punch cannot be energised.
RET (retain) is set by the buffer SU as soon as END is set.
- (vi) Three monostable elements.
PUS DL - When set will remain set for 200 microsec. Simultaneously with setting this delay a ready pulse is emitted to the ESU; the CHB is then filled within 200 /usec.
CLUTCH DL - When set will remain set for 4 millisec. This is set on receipt of a timing pulse from the punch, the punch ready pulse,

which indicates that the 8 punch solenoids may be energised.

CLEAR - this monostable clears the following flip flop registers in the panel buffer.

- (a) UMIS and LMIS
- (b) RET and END
- (c) WR, ERASE, UR1, UR2.

(vii) Punch solenoid drivers - There are 9 of these drivers - one is always active when punching or erasing as it governs the punch-knife punching the sprocket hole - the other 8 which control information channels may only be energised if the CLUTCH DL monostable is set and the ERASE indicator clear.

Operation of the sequence unit

The action of the SU is defined by the 'flow diagram' in fig I1 and also the logical diagrams of the buffer and the sequence unit in Figs. I2 and I3. To perform a transfer, whether the function be a write or an erase, the SU operates as follows:-

- (i) Initially no transfer is being performed and the SU is idling in the loop U000, L000. Before the RSU starts a transfer the buffer is cleared by stimulating the CLEAR monostable.
- (ii) A transfer is set up by the R sequence-unit which sets WR (and ERASE and UR1 as required). As soon as WR is set, the SU tries to perform the main loop as follows:
- (iii) MI's U001 and L001 clear the character buffer, set the PUS DL monostable and emit a ready-pulse to the E sequence unit - this later pulse being a request for information.
- (iv) MI's U011 and L011 constitute a loop causing the buffer SU to wait until the ESU has filled the CHB, and the punch is ready and the tape is not broken
- (v) MI U111 sets the CLUTCH DL monostable thus energising the punch solenoids as required.
- (vi) MI's L111 and U101 constitute a loop whilst the buffer waits for the punch solenoids to act.
- (vii) MI L101 is merely a jump back to step (iii) ready to punch the next character.

When the last character is sent to CHB, the ESU also sets END and thus when the punch has been set up the indicator RET is set. This causes a complete cycle on the buffer SU, without energising the punch, emitting a ready pulse to the ESU which clears the indicator WR and also causes the RSU to complete the transfer by resetting any lock-outs etc:

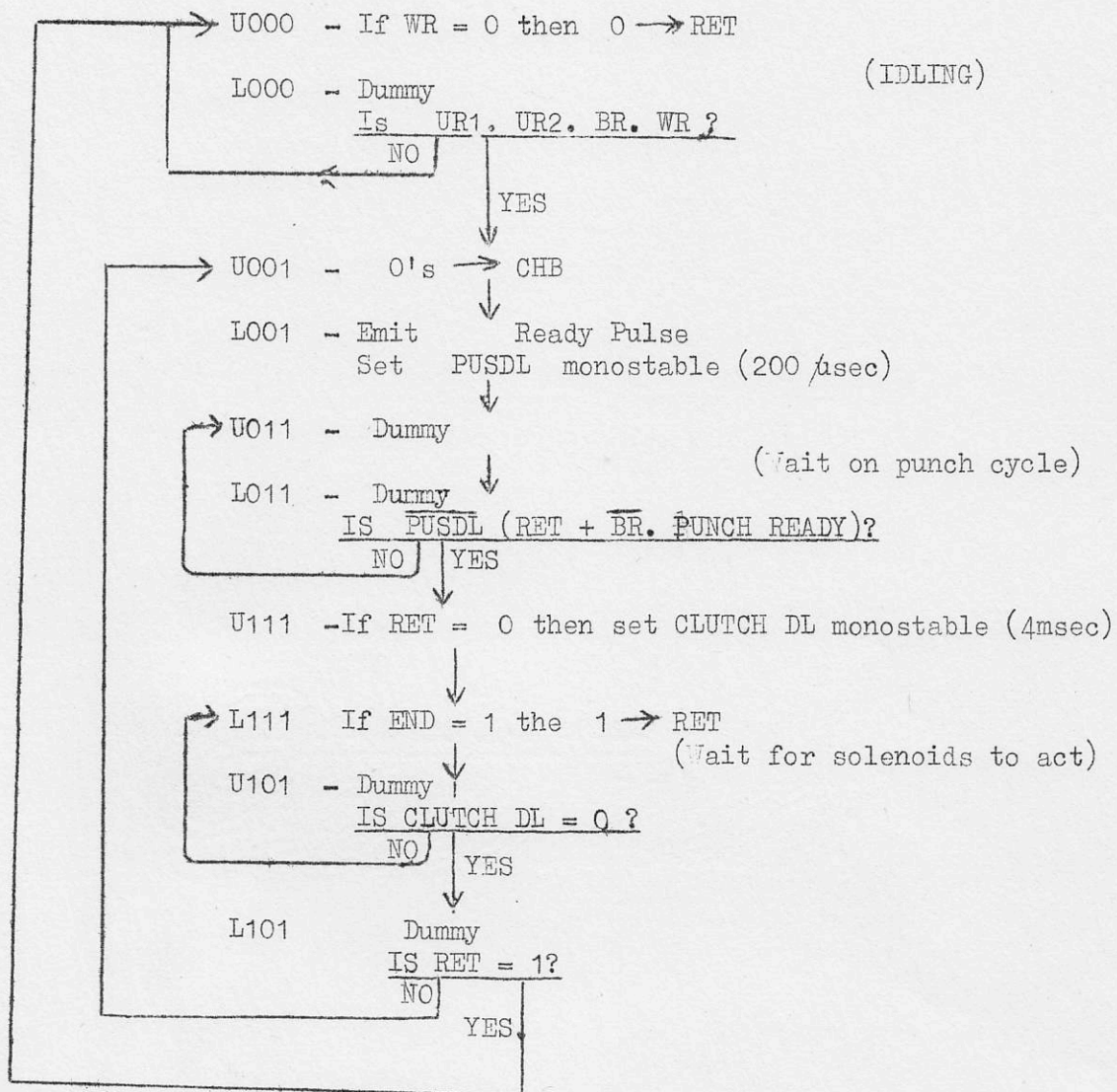


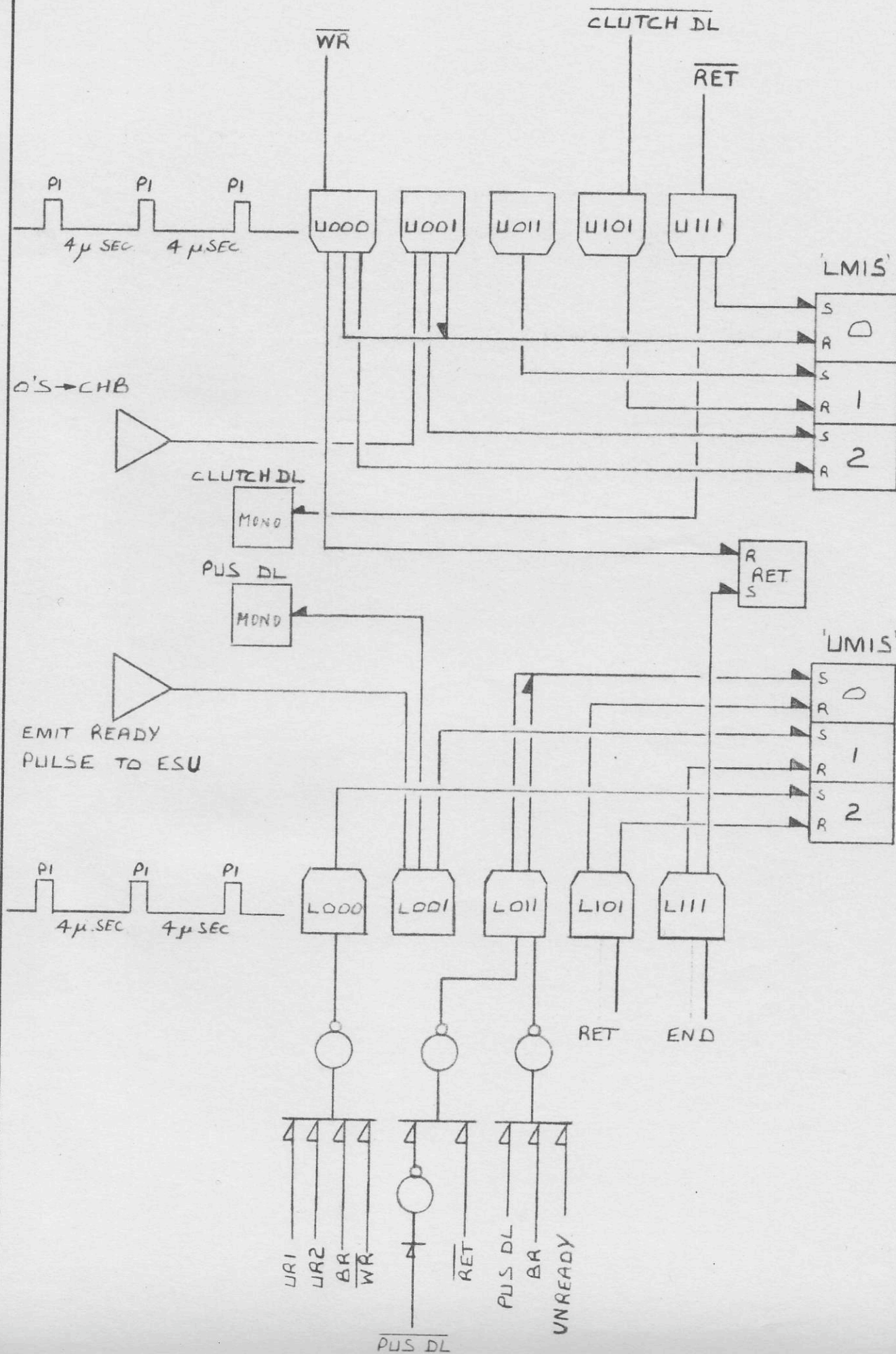
Fig I1 -- Flow Diagram of Paper-Tape punch buffer sequence Unit.

SCHEMATIC OF PAPER-TAPE PUNCH
BUFFER SEQUENCE UNIT.

SHEET NO.:-

OF

SHEETS



SCHEMATIC OF GATING ON SOLENOID DRIVERS
FOR THE PAPER TAPE PUNCH

SHEET NO.:-

OF SHEETS

PULSE FROM ESU

