

'Stay-Put' The Improved Huff & Puff VFO

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THIS DEVELOPMENT of the ideas pioneered by PA0KSB results in an inexpensive VFO of outstanding stability, despite its relatively small number of components.

INTRODUCTION

TO BE ABLE to build a VFO with the simplicity of a Hartley or other L/C configuration, and yet escape the drift problems almost invariably associated with such construction, must have been the dream of most home constructors at some time. The enormous complication of modern phase locked loops and direct synthesis techniques rule out their use in home construction except in very grand projects, even though one might gaze in envy at the stability obtained. The work of PA0KSB, highlighted by G3VA's review [1], led me to offer a simplification [2] of his design, as the stability offered by this relatively simple combination of L/C and digital techniques was outstanding. The general principle of the method seemed straightforward and attracted the light-hearted title of "Huff & Puff", but in truth it is not so easy to understand - witness the hail of letters I received asking "How does it work?" Certainly, one of the best methods of revealing one's ignorance of a subject is to try and explain it to another and the rule surely proved true again in my case. But now, armed with the usual 20/20 hindsight, I wonder what the problem was. The following text describes a low cost and easily built oscillator, with 'rock-like' stability and with some rules on how to vary the design without going wrong.

DOES IT HAVE SHORTCOMINGS?

IN ORDER TO UNDERSTAND the limitations of this type of circuit, first you need to know how it works. The elements of this VFO are:-

1. An L/C tuned oscillator, with limited frequency control by the application of a variable voltage.
2. A high frequency reference oscillator.
3. A circuit to compare these two oscillators.
4. A circuit to remember the result of the comparison (an integrator) and adjust the L/C oscillator accordingly.

The block diagram of such a configuration is shown as Fig 1.

Admittedly this diagram looks like many other phase locked loop type circuits, but it works in quite a different manner. The phase of the L/C oscillator is not locked to the crystal nor is its absolute frequency. In this case the comparator tests whether the frequency of the free-running oscillator is changing relative to the crystal using a time comparison technique, then acts to control the oscillator and hold it steady to within a few Hertz. Thus in this design the oscillator's frequency is never steady but actually dithers about a mean crystal related frequency by 1 or 2Hz. I have calculated the degree of this dither by a combination of oscilloscope measurement and dead reckoning, as it certainly cannot be detected by listening or by measurement using the type of instrument available to the amateur.

HOW IT WORKS

THE VFO FREQUENCY is digitally divided to produce a square wave around 40Hz. The rising edge of this square wave is then compared in time to the rising edge of a high frequency square wave (typically 20MHz) using a device called a D type flip-flop, with the following result.

If the VFO derived square wave (applied to the Clock input of the flip flop) has increased in frequency and rises before the crystal's square wave (applied to the D input), the output of the flip-flop remains unchanged. However, if the D input rises first, the flip flop changes state. Thus, if the VFO is persistently fast, the D flip flop output frequency will be zero, whereas if it is persistently slow the flip flop output will be a square wave at half the clock frequency. If the clock is 40Hz, the flip flop output can vary from 0 to 20Hz, and if the VFO is holding frequency relative to the crystal marker the output will hover around 10Hz. Using this variable frequency to drive a charge pump in opposition to a relatively stable 10Hz feed results in the integrated output voltage of the two pumps increasing if the VFO is slow and decreasing if the VFO is fast. Such a voltage is just right to apply to a varicap and stabilise the oscillator.

SHORTCOMINGS

SO WHAT ARE the shortcomings? Firstly, although this type of control loop will stabilise the oscillator, the exact frequency at which it settles is not under

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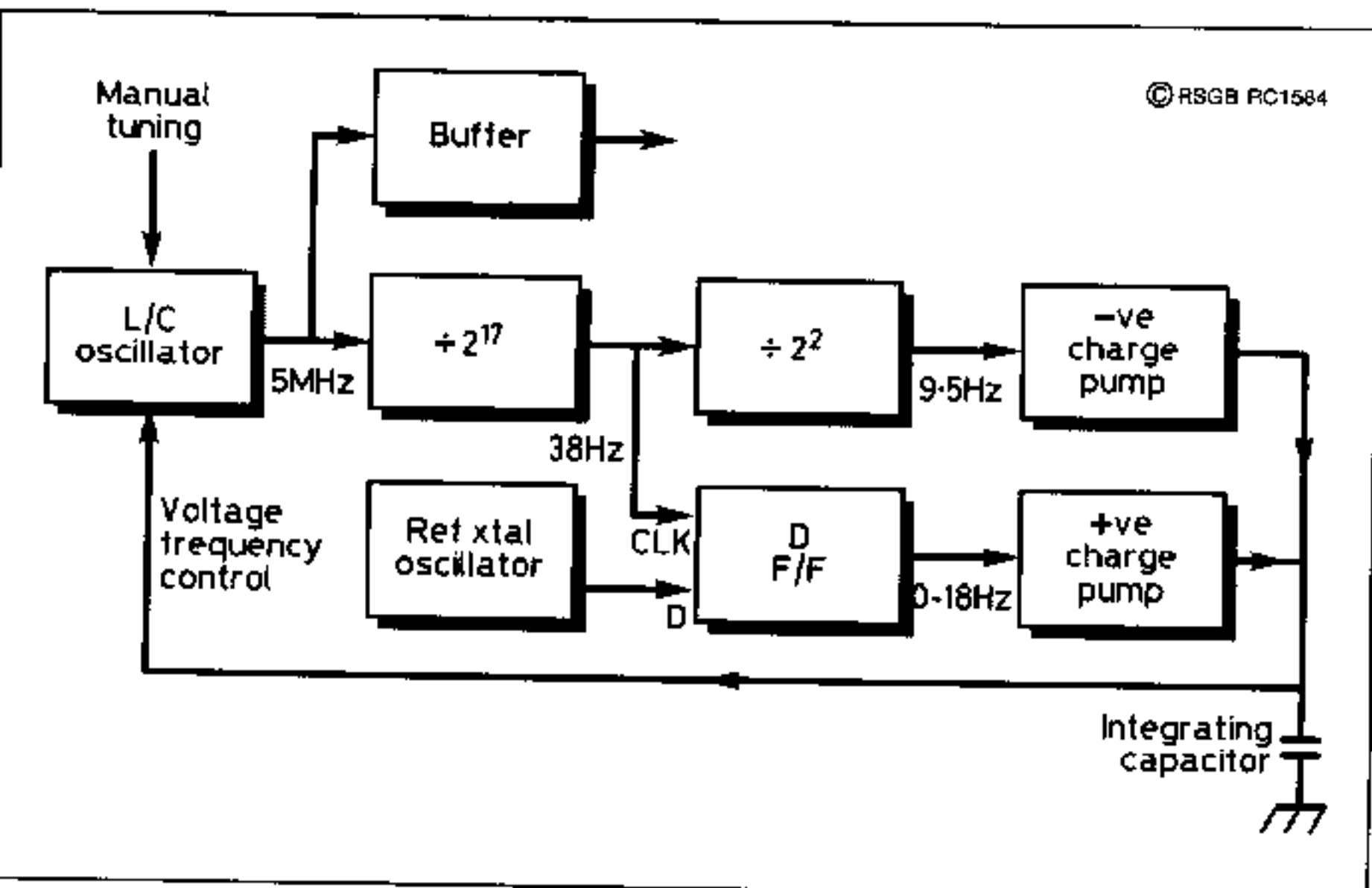


Fig 1: Block diagram of the Stay-put VFO.

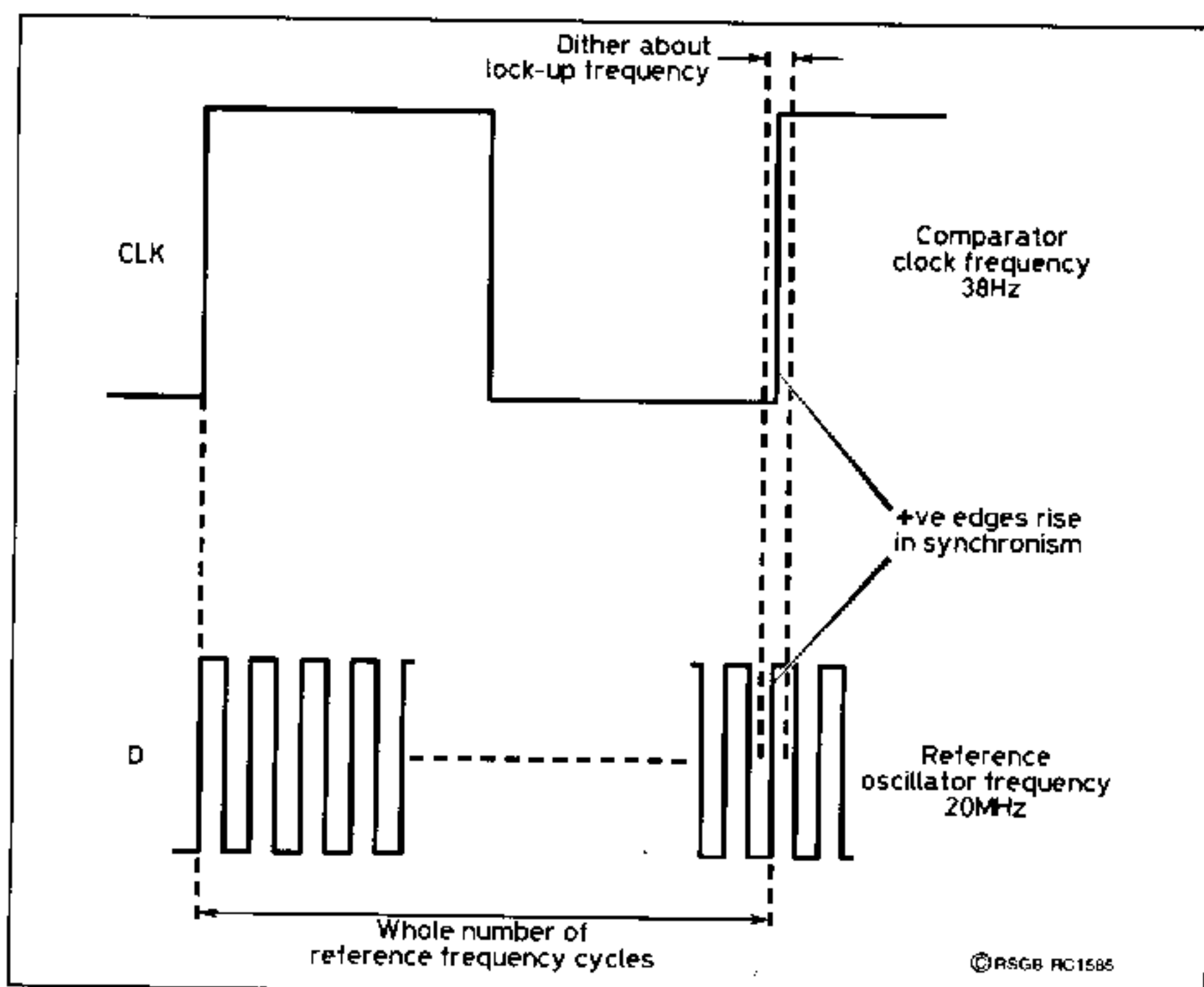


Fig 2: Timing diagram of the D-type Flip Flop.

73 the users control! As soon as manual tuning stops, the control loop moves the frequency to the nearest lockup point. This idea may be appreciated more easily by reference to Fig 2, which shows the two input trains to the comparator. The control loop will only settle when the rising edges of waves 'Clk' and 'D' are coincident, and clearly, the smallest change possible in the period of wave 'Clk' is plus or minus one period of the reference wave 'D'. In the early designs [1] [2], comparison frequencies around 300Hz were used which resulted in lockup frequencies some 150Hz apart when using a 40MHz crystal. This is just about acceptable for CW but a bit rough for SSB. Even my own (improved!) effort had a 76Hz gap between lockup points. The VFO was undoubtedly stable, but only on its own terms.

A further problem was that overtone crystal oscillators working above 20MHz tended to be a little touchy when built around digital ICs and could not be described as reliable.

Both these difficulties are tackled in the present design. The frequency step between lockup points has been reduced below 10Hz, and a crystal oscillating in fundamental mode

at around 20MHz - sure-fire with ICs - simplifies the reference oscillator.

TECHNICALITIES

THIS STABILISER is intended to react against long term drift in the VFO. It is therefore necessary to define what is meant by frequency drift in this context, as tuning the VFO could be seen as rapid drift. For this design, which is a 5MHz oscillator, the primary design parameters are:-

- 1. The maximum uncompensated drift rate should not exceed 200Hz per minute and total uncompensated drift over a 30 minute period should not exceed 750Hz.
- 2. The varicap should be capable of changing the VFO frequency by around 2 to 4kHz (not critical), for a change of 1 to 6 volts applied. At around mid control range, ie 3.5 volts, it should move the VFO by about 400 to 600Hz per volt.
- 3. The integrator maximum slew rate = 1 volt per minute.
- 4. Lockup increment = 9.5Hz (approx)
- 5. Crystal frequency = 20MHz (approx)
- 6. VFO wander after lockup = ±2Hz

MATHEMATICS

THE RELATIONSHIPS BETWEEN the VFO, crystal and comparator frequencies is established by the following formulas:-

Tuning increment:

f(inc) = f(vfo) - (2^n / (f(vfo) + f(xtal)))

Comparator frequency:

f(comp) = f(vfo) / 2^n

Number of crystal cycles per comparator period:

N = f(xtal) / f(comp) = f(xtal) x 2^n

Where f(inc) = frequency increment between lockup points; f(vfo) = vfo frequency; f(xtal) = crystal frequency; f(comp) = comparator frequency; n = number of divider stages; N = number of crystal cycles per comparator period.

Even though the formula for the frequency increment is 'straightforward', as the mathematicians might affirm, it is to say the least unwieldy. One can, however, calculate the numbers with a little reasoning and only the simpler formula, as illustrated by the following example.

With a VFO running at a nominal 5MHz and using a 17 stage divider, the comparison frequency is:

f(comp) = 5 x 10^6 / 2^17 = 38.14697266Hz

Thus the number of crystal oscillator cycles (20MHz xtal) to one of the comparison frequency is:

N = 20 x 10^6 x 2^17 / 5 x 10^6 = 524,288

So we get 524288 positive going edges on

the D input of the comparator for one at the Clock input. If the VFO frequency is increased, the next possible lockup point will be with 524287 periods of the reference frequency (ie 1 less than before), equivalent to:

f(vfo) = 20 x 10^6 x 2^17 / 524287 = 5,000,009.537Hz

Subtracting the original frequency from this gives a minimum frequency increment of 9.537Hz.

This calculation is based upon a crystal reference of exactly 20MHz. However, the exact crystal frequency is of little importance, for if one used an 18MHz crystal the above calculation would show an increment of 10.587Hz.

Finally, the sharp eyed may note that the values of f(inc) and f(comp) depend upon the absolute VFO frequency. Thus the tuning increment varies with the VFO frequency. A little arithmetic will show that shifting the VFO by 100kHz will increase the step size by 0.19Hz, which is of no practical significance.

THE CIRCUIT

THE COMPLETE CIRCUIT is shown in Fig 3. A separate VFO is unnecessary, as the HC4060 IC has two gates intended for use as an oscillator. The tuning circuit is in the form of the pi network C5, C6 and L1. The main tuning capacitor, VC1, in parallel with C5, is a small receiving type of value 150pF. It provides a tuning range of just over 100kHz, centred on 5MHz, but may easily be varied to suit (see later). VFO output is taken from pin 9 of the 4060 (IC1) and passed via three HCU04 buffers in parallel, (half of IC4), to an output attenuator which provides a VFO output of just over 100mV RMS from a 50Ω source. A second 4060 (IC2) is used to complete the divider chain, the two outputs being pin 7 (38Hz) and pin 4 (9.5Hz). The reference oscillator uses the other half of IC4. The first inverter makes an oscillator which is sure-fire with crystals in fundamental mode. The second and third inverters buffer and square the reference output.

The comparator uses half of an HC74 (IC3), the unused half having its inputs tied positive for stability.

The complementary charge pump circuits TR1 and D1, plus TR2 and D2 are driven directly by the HCMOS devices. The combination of the pump capacitors C1 and C2, together with the integrating capacitor C3, produce an increment of near 2.5mV per input pulse, which translates to just under 1Hz change in VFO frequency (not easily detected!). Resistors R1 and R2 fix the reset voltage for the integrator at around mid range, ie 3.5V. A stable six volt supply is essential. The regulator Reg 1 supplies the 50mA required by the circuit.

Apart from setting L1 to the correct frequency, there are no adjustments to be made. . . unless of course you don't wish to have a VFO on 5MHz or would rather control an existing VFO. More on this later.

CONSTRUCTION

IDEALLY A SMALL PCB should be used, and my own effort went onto a piece of copper clad board just under 2in x 3in. There is only one tricky track, the ground lead from IC1 pins

COMPONENTS	
Resistors	
0.25W, 5% tolerance, carbon or metal film	
R1	3k3
R2	4k7
R3	560k
R4	1k
R5	240R
R6	1k
R7	680R
R8	56R
R9	10k
Capacitors	
C1, C2	470p 160V polystyrene
C3	1µ 16V Tantalum
C4	18p 160V polystyrene
C5	820p 160V polystyrene
C6	470p 160V polystyrene
C7, C8,	
C13, C14	100n polyester
C9	47µ 16V Tantalum
C10	33p 160V polystyrene
C11	22p 160V polystyrene
C12	47p 160V polystyrene
Semiconductors	
D1, D2	1N4148
D3	MV2102 or BC182 (see text)
TR1	BC212
TR2	BC182
Reg1	LM317T
IC1, IC2	74HC4060
IC3	74HC74
IC4	74HCU04
Additional items	
X1	20MHz HC6U type
L1	TOKO KANK 3334R
VC1	Small airspaced 150p receiving type variable
Component Suppliers	
Small twin gang tuning capacitor	
J Birkett, Lincoln. Tel 01522 520767.	
Surplus HC6U crystals	
Keytronics, Bishops Stortford. Tel 01279 505543.	
TOKO inductors	
Circuit Distribution Ltd, Broxbourne. Tel 01992 448899.	

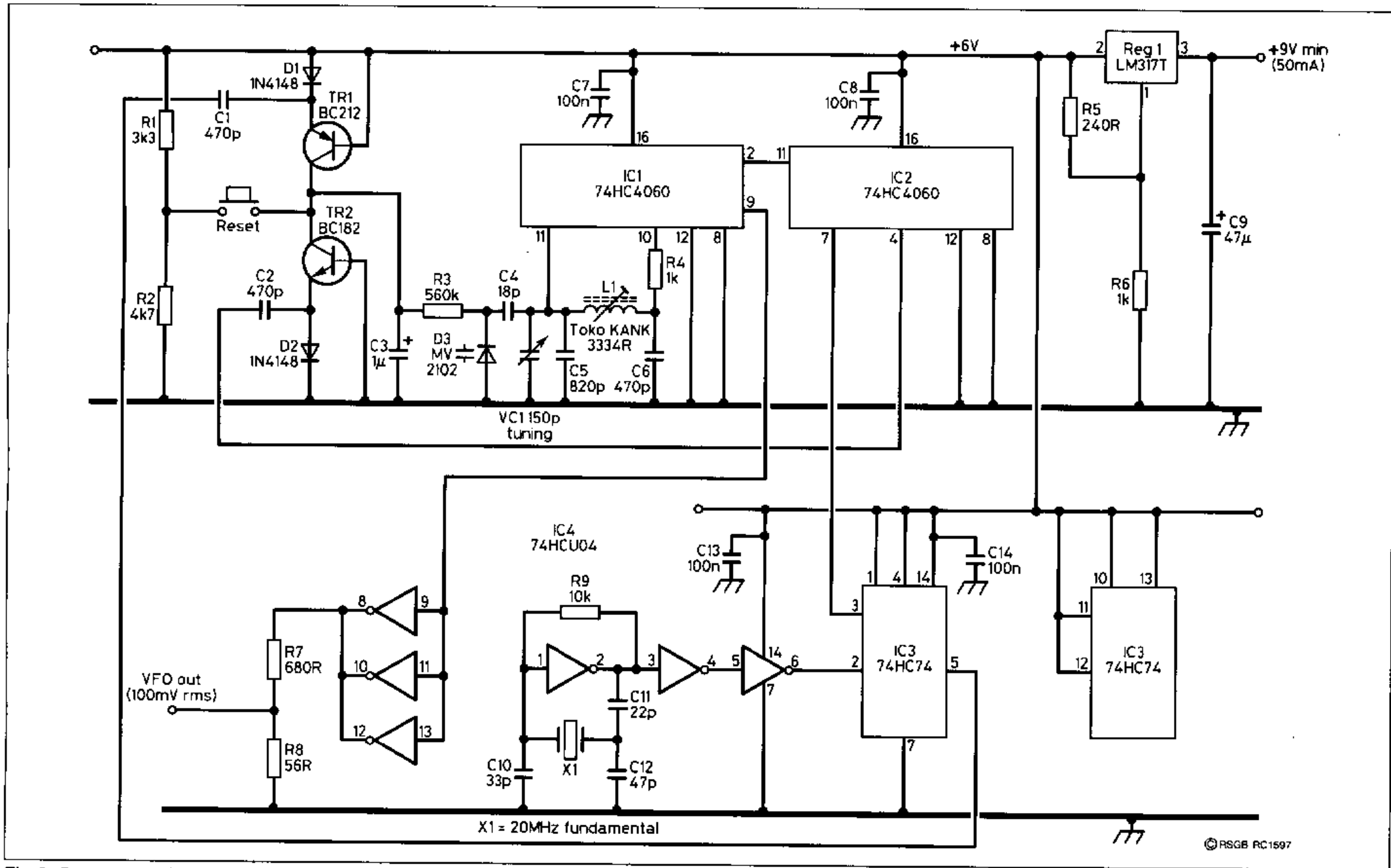


Fig 3: Stay-put VFO schematic.

8 and 12. If you find this squeeze unacceptable, a short jumper lead is easily accommodated. There are already four wire links above the board, coded P, Q, R and S. The connections to the RESET switch are coded T. The fixed vanes of the tuning capacitor connect to point V. The prototype was built with the PCB soldered to the frame of the tuning capacitor, which is why no ground connection for VC1 is shown. If the tuning capacitor is remote from the board, I recommend using miniature coax for the connection. An extra Vero pin could be inserted in the ground track adjacent to pin V to take the screen.

A good many of the IC's pins are unused and no holes are drilled to accommodate them. These unused pins are easily bent up to clear the board. Earlier experimental versions were produced ugly style on the surface of the copper-clad board. As long as the leads are short and well fixed, the performance is the same.

I find it worthwhile to ground the metal can of the crystal as it adds a little to stability. There are plenty of surplus HC6U style crystals available in the 20MHz region. Remember, the exact frequency is of no importance, as it only changes the incremental step frequency by a tiny amount.

VARIATIONS

DURING DEVELOPMENT of this VFO, conversations with G4GVM, and correspondence, drove home the revelation that the rest of the amateur radio world did not necessarily share my own obsession with 5MHz VFOs tuning 100kHz segments. Thus I offer the following points for consideration by those ploughing different furrows.

To increase the tuning range, use a larger tuning capacitor in place of the 150pF that I specified. If that is still not enough, connect the tuning capacitor in parallel with C6 (470pF)

instead. I do not recommend reducing the values of C5 and C6 as the inherent stability of CMOS oscillators of this type is not good unless well loaded with capacitance. Tuning capacitors are expensive and I tend to use small twin gang air spaced receiving types, which commonly have values between 150pF and 300pF. It is easy enough to vary the effective tuning capacity by series and / or parallel fixed capacitors, and much more economical than buying special components.

The inductor used (L1) is a standard TOKO component.

To build an oscillator for 3.5 or 1.8MHz I would reduce the number of divider stages in use by IC1, so that the comparator clock frequency is maintained around 40Hz. This is easily done by selecting a different output from IC1 (pins 1, 2 or 3). Pin 1 output is more suitable for frequencies below 5MHz and Pin 3 for 7 or 9MHz.

The C5, L1, C6 tuning circuit is arranged to hold the voltage swing on the varicap diode to around 1 volt peak to peak and I would advocate the two to one ratio between C6 and C5 be maintained, even if the absolute values are changed to suit other operating frequencies. Remember, this VFO is proof against slow drift but cannot do anything to compensate for fast changes in frequency, no matter from what cause. Hence good construction practice must be followed for the best results.

The varicap diode I used was an MV2102, which is a small capacity type (8pF at 4V). Only a very small change in capacity is needed, as the tuning range provided by the diode only needs be 2 to 3kHz for a control voltage change of 1 to 6 volts. I recommend that you test the diode you intend to use by varying the control voltage across C3 using a potentiometer and measure the actual frequency change. If it turns out to be greater than 3kHz, try reducing the value of C4 before replacing the diode. Alter-

natively, try using something like the base-emitter junction of a BC182 as the varicap diode (base to ground, ignore the collector). The one I tried was ideal and pulled the VFO about 2.4kHz. The point of this exercise is that too big a pull by the varicap will increase the random shift in the VFO frequency when locked due to the step noise inherent in the charge pump and which in extreme cases could prevent proper lockup.

The case of an existing VFO with drift can be easily tackled. Firstly remove the oscillator components C5, C6, R4, L1 and VC1. Disconnect C4 from pin 11 of IC1. Connect a 470kΩ resistor between pins 10 and 11 of IC1 (DC bias for the input buffer) then feed pin 11 from a low impedance point in your existing VFO via a 22pF capacitor. Only around 250mV of drive is necessary. If the VFO provides much more than this, reduce the drive to IC1 by adding a resistor in series with the 22pF capacitor.

Reconnect C4 to the tuned circuit of the oscillator. Try using the emitter tap on the coil or capacitive tap if a Colpitts type, and experiment with the frequency shift obtained when changing the varicap control voltage over its full range (1 to 6 volts). Remember, it only needs to pull the oscillator by 2 to 4kHz maximum. Reduce the value of C4 if necessary.

CONCLUSIONS

As mentioned previously, the only adjustment needed is to set the core of the tuning inductor to bring the VFO into the correct frequency range. However, after constructing a complex circuit it is comforting to be able to make a few measurements just to see that all is well. The following remarks are intended to give the constructor a feel for what to expect. At switch-on both oscillators should come to life. A solid 5 to 6 volt square wave at the crystal's funda-

THE STAY-PUT VFO

mental frequency should be observable at pin 6 of IC4. The VFO should operate no matter what control voltage is applied to VC1, and a good 300mV peak to peak should appear at the output. Assuming the VFO is operating around 5MHz, square waves of 38Hz and 9.5Hz should be observable at pins 7 and 4 respectively of IC2. The amplitude of both should be near 6 volts peak to peak. The output at IC3 pin 5 will look unstable and have a varying frequency in the range 0 to 18Hz.

So far, so good, but to check that the charge pump is working correctly requires a little caution. This is a very high resistance circuit and applying even a 10M Ω oscilloscope probe to C3 in an attempt to measure the control voltage will disguise the true state of affairs. One needs to use the buffer circuit shown in Fig 4 for this purpose. Using a common FET like the 2N3819 allows measurement of the voltage across C3 without taking any current from the circuit, but you need to be aware of the offset voltage added by the FET to the result measured across its source resistor. This offset is established by shorting the FET's gate to ground. The voltage at the source is then the offset which must be subtracted from any readings subsequently taken.

When this is done, briefly put a short circuit across C3, remove it, and then short circuit D2. The voltage across C3 should slowly build at about 1 volt per minute, indicating that TR1 is working. This being so, remove the short circuit from D2 and place it across D1. The

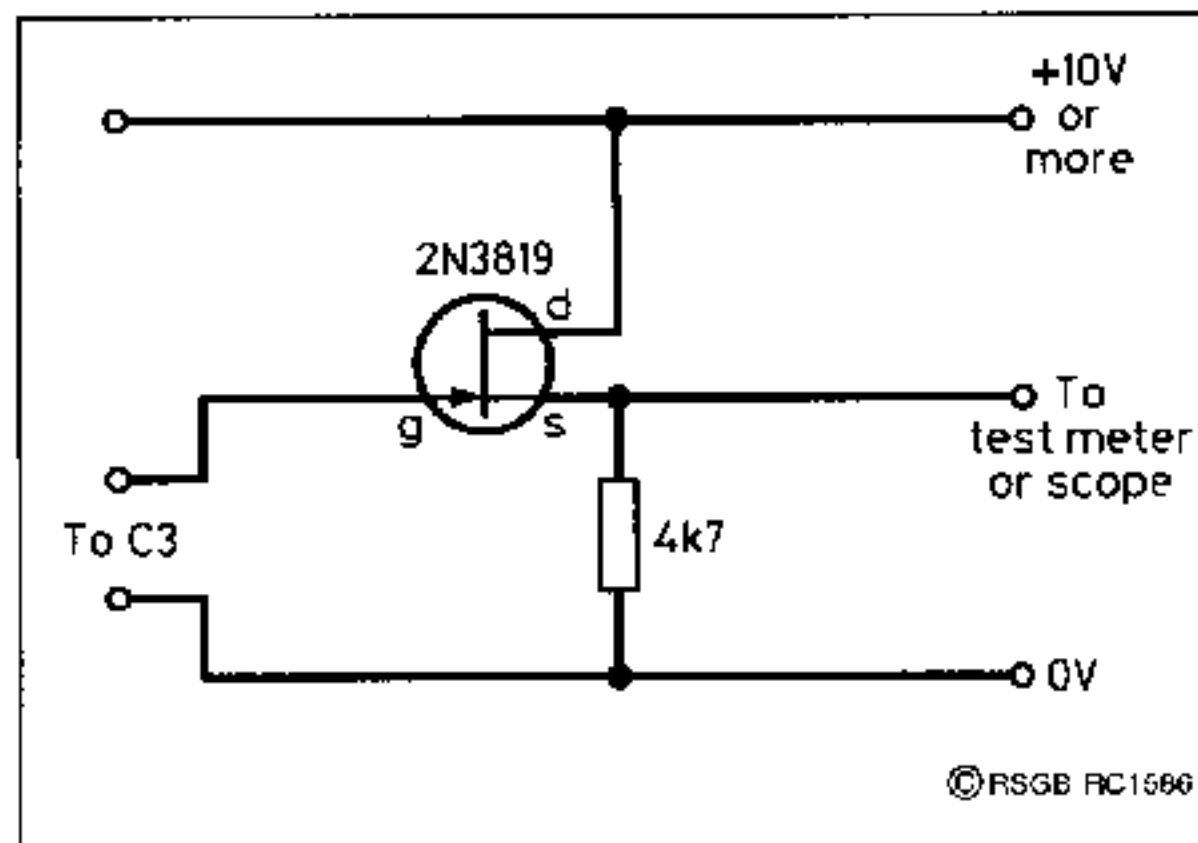


Fig 4: Charge pump test buffer.

voltage across C3 should now slowly decrease, showing that TR2 is working. If all the foregoing is true, then remove the short circuit from D1 then press the reset button to set the control voltage to mid range. In the lockup condition both pump frequencies will measure the same and observation of the FET buffered voltage on C3 will show a steady DC voltage with 2mV steps superimposed upon it as the control loop regulates the frequency.

In operation I use the following drill. Switch on and leave the VFO alone for maybe half a minute to allow any initial rapid drift to settle, then press the reset button. Tuning is now as any other VFO. The reset button is unlikely to be needed again at intervals of less than maybe 30 minutes. When first this circuit is put into operation, one is usually curious as to just how long a period can elapse before a reset is needed. If the test FET buffer (Fig 4) is initially

left in circuit, the time taken for the integrator to 'hit the rails' can be established. A well-built model can go for hours without needing to be reset. My own practice is to press the reset button at the start of each new QSO - if I remember.

Interestingly, tuning up and down the band causes little change to the voltage across C3, the control voltage, as such rapid changes in frequency cannot be followed by the drift compensator circuit. Similarly, if the VFO frequency is shifted by 800Hz or so on changing from receive to transmit in a transceiver, the stabiliser will ignore this shift also. This was a matter of some amazement to me when I applied this circuit to my station's homebrew multiband transceiver, but as the months have gone by I now accept it as normal!

PCB

The PCB layout is available from the author by sending a stamped, self addressed envelope, or from the RSGB website www.rsgb.org/news/radcom/stay-put.htm

REFERENCES

- [1] 'Technical Topics', *RadCom* July 1996 (Note correction in Technical Correspondence, *RadCom* August 1996)
 - [2] 'Technical Topics', *RadCom* September 1996.
- [See also 'Technical Topics', *RadCom* December 1997 - Ed]. ♦