

More views on huff and puff VFOs

This seems to be time to turn to a report from John Compton, BRS33886, of Southampton who, like Joe Cropper, G3BY, (*TT* October) has tried out the system for what seems a very practical application—improving the stability of an existing receiver.

He makes the point that inherently the system (“brilliantly simple”) is “a lazy man’s answer to a problem which, as G3PDM has shown (*TT* December 1969 and *ART* 3 and 4), can be solved by more conventional means.” In other words, if you are starting out to build a good vfo you can achieve good stability without stabilization if you take the type of precautions outlined by G3PDM, or alternatively think in terms of a *good* frequency synthesizer. But on the other hand, as BRS33886 states, “to someone who wishes to improve an already-built or commercial receiver or transmitter without major internal changes the idea is certainly promising.”

And this was the basis of his own experiments: using as the test bed his FR400 receiver with a vfo which normally drifts some 1,900Hz from cold and tends to be still drifting at a rate of 280Hz per quarter-hour after one hour’s warm up, no matter how the thermal compensation adjustments provided on the receiver are adjusted. After adding stabilization the total drift from switch-on was less than 60Hz and was at no time faster than about 1Hz/min; and this drift could possibly be attributed to the temperature coefficient of the timing crystal which is not in an oven.

BRS33886, like G3BY, emphasizes that the original simplified block diagram, reproduced in *TT* from *Reflecties* (*Electron*) is a little misleading but the amendments needed in practice are fairly obvious; similarly he believes that something went wrong in the presentation of the “timing periods” since these appear to be calculated on a decimal basis rather than divide-by-sixteen: a gate-open time of 1s gives 16Hz increments; 0.4s 40Hz, and so on.

“It is quite unnecessary,” he writes, “although sometimes convenient when using clock pulses derived from other equipment, to use a long gate-closed period. Several microseconds only are needed to store the counter output, zero the counter and open the gate—so that the device can be active for a larger proportion of the time, so improving resolution. For convenience, I have used a gate-closed time of 1/128th of the clock period, derived from seven of the inputs of a 7430 8-input nand gate fed from the last two divide-by-sixteen ICs in the clock pulse generator, giving a clock period of about 0.5s, found to be about optimum.”

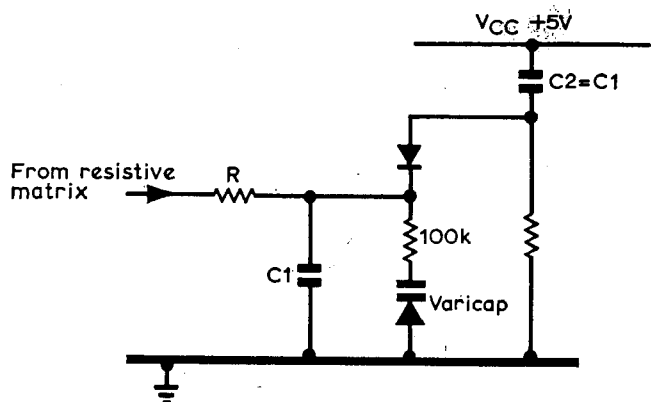


Fig 1. BRS33886's suggestions for roughly stabilizing voltage across the frequency compensating varicap to reduce the time needed for the huff and puff stabilizer to take effect after switch on

I used a 7493 counter (cheaper than 74141 but asynchronous) set to divide the vfo frequency by eight. A simple fet/pnp-bipolar/7413 amplifier/shaper was used to match the 5MHz vfo output to the ttl levels, giving an increment of about 16Hz, which seems closer than really necessary; 32Hz or even 64Hz would do very well."

He tried a proportional output voltage by using a resistive matrix (1k Ω , 2.2k Ω and 4.7k Ω from the $\div 8$, $\div 4$ and $\div 2$ outputs of the counter) using a 7475 quad-latch in place of the 7474. While this works, he doubts if the refinement is really helpful, although perhaps worthwhile if the basic oscillator showed fast or erratic drift.

A difficulty is that of reset accuracy after switching the equipment off for a time; some network is needed to ensure an approximately correct voltage across C1 when switching on. Fig 1 works well, but the voltage across C varies considerably after a switch-off/switch-on sequence, resulting in a frequency shift of up to 2kHz (in this particular example). This is perhaps of little practical importance for most amateur applications; no obvious solution has been discovered.

If most of the range of output voltage is to be used for frequency compensation (from almost zero to about 4V), a two-varicap circuit is needed to eliminate conduction of the varicap at low control voltages which can result in a flattening or even reversal of the voltage/frequency characteristic. Fig 2 shows a two-varicap arrangement.

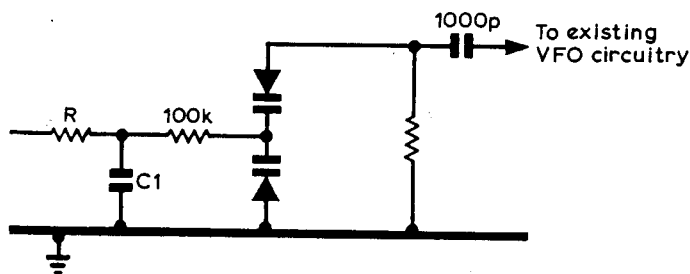


Fig 2. Use of two variable capacitance diodes to make fuller use of the full range of control voltage

Some care has been found to be needed in determining the best point in the existing circuitry to connect the compensating element. There is no point in connecting the circuitry directly across the vfo inductor if this results in, say, 100kHz shift for 0 to 4V variation when possibly only 2 or 3kHz drift is expected. Series and/or parallel padding

and trimming capacitors may be needed to get the right degree of compensation, or a less sensitive point may be found in the existing circuitry, as is possible in the FR400.

Values and ratio of R and C1 appear to fairly non-critical. BRS33886 found 220k Ω and 2,000 μ F suitable. He suggests that a simple technique is to use an available capacitor and then try increasing values of R until a value is reached which has no overshoot. BRS33886 does not feel that a special low-leakage electrolytic is really necessary for C1 provided that the leakage is reasonably constant. He found that low-cost electrolytics all worked quite well. Although a tantalum type might let the circuit settle down rather quicker, he finds it takes only about 45s with lower cost capacitors.

On the assumption that the function of the first PA0KSB 74121 was to ensure that no switching took place before the gate was closed, BRS33882 replaced this with a 100 Ω , 1,000pF integrator, inverted the sign of the input pulse and used the B input to the second 74121; this works quite well and it is possible that the other 74121 circuits could be replaced using a couple of spare gates, but this has not been tried.

A side effect of working on the system has been the large number of spuri; these are not prominent at hf but of considerable potential nuisance value at vhf, and enclosing the added circuitry in a die-cast box remote from the receiver, and with its own battery power supply, did little to improve the situation. The spuri arise mainly from harmonics of the 5MHz vfo and the various clock frequencies (these can, of course, also be a problem in almost any form of digital frequency synthesizer). It has not proved possible to eliminate them at vhf; this could prove a major problem for vhf applications.

BRS33882 emphasises that despite his comments and reservations he nevertheless feels the idea is ingenious and practicable—with the possibility that a single add-on unit could be used with a number of separate receivers and various vfo frequencies at an extra cost of possibly a plug and a couple of diodes per vfo. Using the stabilizer on his FR400 receiver has made operation much easier, especially for weak and fading signals, and he says, "It's great being able to switch on two minutes rather than two hours before a specially wanted transmission—if only transmitter frequencies were equally stable!"

Finally before leaving this subject (which seems well worth the space since it concerns a matter affecting almost everyone), a quick comment from Dave Martin, G3RUZ. This refers to G3BY's point about using external resistors with the 74121 devices. He says this device has an internal 2k Ω resistor which may be used in cases like this (where the length of the output pulse is not critical) by simply connecting together pins 9 and 14 of the ic.