

920M MCM7 Update

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Between January 2023 and February 2024,
I produced various files describing the Elliott 920M MCM7.
This file provides minor updates to several of those files,
and significant corrections to LOGICSUB.PDF & EXPLANAT.PDF.

On INTERFAC.PDF 4th page: prefix the title
"20 Plug C, Application Interface" with a "9".

According to AP 101B-3101-10KB1 chap 71-10 page 80 (page 88 of 124):
my PLA/37 "StoreOther" should be "~SUT" = "~StoreUnderTemp",
my PLA/54 "StoreReady" should be "~SOT" = "~StoreOverTemp",
and so my "~StoreReady" should be "SOT" = "StoreOverTemp",
and both PLA/37=U1/31 & PLA/54=U1/32 are indeed seen normally high.
Incidentally, I've noticed that the AP does contain some errors.

In my EXPLANAT.PDF, I noted that my WIRING.PDF was derived from
MCM7 5343 and was checked against MCM7 88, but that the derivation
of CON-CIRC.PDF & REG-CIRC.PDF from WIRING.PDF was not entirely
automated. Since then, I've desk-checked WIRING.PDF wire-by-wire
against CON-CIRC.PDF & REG-CIRC.PDF and have found no discrepancies.
It remains the case that, should there be a conflict, WIRING.PDF
is the more trustworthy. Sadly it also remains the case that it is
sometimes hard to spot that a signal generated and used on one page
of the circuits might be used on other pages, as is often the case.

LSA type -G? is -84

In early 2025, I had the opportunity to inspect a further six MCM7
machines. I now know that the LSA which I have called a "type -G?"
is actually a "type -84". This name appears in CON-DECK.PDF, on
the Reset & Timing page of CON-CIRC.PDF, and in one paragraph
of LOGICSUB.PDF (which now places it out of alphanumeric order).

LSA types -80 and -81

As stated in LOGICSUB.PDF, the only LSA type -80 is at A26
and the only LSA type -81 is at A51, both on the register deck.
They appear within the wiring which shifts the A-register
left 7 places when paper tape is read, and they both just
contain links between various pairs of pins.

LOGICSUB.PDF's description of the links inside these LSAs is correct
(except that my comment that the A26/01&13 link was unused was wrong),
but I have discovered that all 15 pins (including what are usually the
power pins) of deck slots A26 and A51 are connected to data signals:

```

n/c A26/15=~Reader06=A23/09
n/c A26/14=~Reader07=A29/09
B05/12=~Areg01=A26/01 ==> A26/13=~Reader08=A40/09
B08/13=Areg02=A26/02 ==> A26/12=Reader09=B32/12
B08/12=~Areg02=A26/03 n/c
B11/13=Areg03=A26/04 ==> A26/11=Reader10=B41/07
B11/12=~Areg03=A26/05 n/c
B14/13=Areg04=A26/06 ==> A26/10=Reader11=B44/14
B19/13=Areg05=A26/07 ==> A26/09=\
                        /=A26/08 n/c Reader12=B47/11
B22/13=Areg06 n/c A51/15=/
                        \=A51/01 ==> A51/14=Reader13=B50/14
B25/13=Areg07=A51/02 ==> A51/13=Reader14=B54/05
B28/13=Areg08=A51/03 ==> A51/12=Reader15=B58/11
B31/13=Areg09=A51/04 ==> A51/11=Reader16=B61/10
B40/13=Areg10=A51/05 ==> A51/10=Reader17=B64/12
B43/13=Areg11=A51/06 ==> A51/09=Reader18=B66/10
B46/13=Areg12=A51/07 n/c
B49/13=Areg13=A51/08 n/c
```

Those signals which are linked by LSAs -80 & -81 and are marked "====>" above are currently shown in WIRING.PDF; most connections marked "n/c" are not yet in WIRING.PDF. My suggested swapping of the two LSAs would do nothing useful.

The diagram above shows that input from Areg06 and output to Reader12 are wired to both slots, so different LSAs could implement 5 or 6 (but not 8) place shifts. The wiring also permits some combination of ORing from bits 1 to 3 onto bits 6 to 8, in the way that bit 1 is currently ORed to bit 8. Perhaps LSA types -82 & -83 would have given a 5-place shift.

LSA type 502 versus 562

As stated in LOGICSUB.PDF, the only LSA type 502 is at E28 on the control deck, and it appears to be identical in function to an LSA type 562, which provides four 2-input Nand Gates using a single 946 chip, and also contains a capacitor.

I removed the 502 from E28 on machine 5343, and found that it contains two 932 chips and a capacitor. Each 932 provides two 4-input Nand Buffers, so the type 502 is simply a high fanout version of a 562. This could have been implemented using a single 957 "quad two-input buffer", but 957 chips are not used elsewhere.

So in CON-CIRC.PDF, the depiction of all four E28 gates should be changed from "&" to "Buf". It is not clear which of the four gates requires a high fanout. E28/02 drives three loads and the other three outputs drive one load each.

There is also LSA type 563, which provides two 2-input Nand Gates and 2-input & 3-input Nand Buffers, which might have been used if at most two buffers were needed, but this has a different pin-out.

The wiring of LSA type 562 is marked "T62" whereas the wiring of LSA type 502 is marked "T502", suggesting that 502 is the later design, probably introduced to solve some timing problem, without redesigning the deck.

LSA types 551 and 552

My description of the operation of the two-stage latches, LSA type 551 used for the A,Q,J,C registers and LSA type 552 used for the M register, in LOGICSUB.PDF & EXPLANAT.PDF, is wrong.

I said that their input bistable is set low by the global Phase1 clock on their CLR pin, then their input bistable can then be set high by unclocked data gated by the Primary Gating Signals; and that their input bistable is transferred to their output bistable by a Secondary Gating Signal on their CLK pin which occurs on the Phase2 clock.

This was based on the observation that, whilst most input data is available before & during & after the Phase1 clock, the data from the (Internal or External) Store, or from Initial Instructions (strobed by a store signal) does not arrive until some time later.

The Phase2 & Phase1 pulse appear close together in that order, so it was only possible to decide what the fall of Phase2 versus the rise of Phase1 did, by removing and testing a 551 & 552 from machine 5343. Whilst doing this, I realised that the way a 552 treats the above Store signals differs from other inputs.

In LSA type 551, the Phase2/CLK input clocks the data, from any of its various sources or nowhere, into the input bistable, and the Phase1/CLR signal transfers it into the output bistable. In LSA type 552, the Phase2/CLK input clocks the data, only from the hand keys or the adder or nowhere, into the input bistable, and the Phase1/CLR signal transfers it into the output bistable. Low data from either Store, or high data from Initial Instructions, can subsequently pull just the output bistable high (the input bistable of a 552 is not visible externally).

So the names CLR & CLK which I have given to some pins on LSA types 551 & 552 in LOGICSUB.PDF & EXPLANAT.PDF is inappropriate, and my depiction of LSA type 552 in LOGICSUB.PDF & REG-CIRC.PDF is wrong: the input from pins 4,5,6,7 (and 3) should be separated from the input from pins 11,12,13: they should not be wire-ORed together.

The Phase1 clock lets the register "slow" outputs take on their new values from the previous cycle, by transferring them from the input bistable to the output bistable, then there is a delay whilst data goes via the adder (and its carry chain) back to the register inputs, where they are clocked into the "fast" outputs by Phase2, and can be safely used immediately outside the highway loop.

LSA type 553

It is possible that each LSA type 553 puts 4 loads on input pin 11. If so, there are 28 loads on buffer output E26/10, "tP".

LSA type 560

My description of the operation of the counter adder, LSA type 560, in LOGICSUB.PDF & EXPLANAT.PDF, is wrong. It has a Reset input, suggesting that it contained a latch, reinforced by the incorrect belief that the attached 551s were cleared by a Phase clock and so the microprogram count value must be held in the 560s at that point.

The chain of six 560s takes the current microprogram count from the 551s, adds one it, provided SuppressCount & CycleRept are both false, and presents it as an input back to the 551s. It was not clear exactly what the 560s did without removing one from machine 5343 and testing it.

Input "In" on pin 6 is inverted and output as "~Out" on pin 5. Input "~In" on pin 9 is inverted and output as "Out" on pin 8. They are independent: they not interconnected as a bistable, although when in circuit, they act as expected. They output the current count value, not the next one, to the counter decoders. Input "In" on pin 6 and "Cin" (CarryIn) on pin 11 are also used to calculate the next counter value: "Cout" (CarryOut) on pin 13 and "+" (AdderToCounter) on pin 2.

This leaves the mysterious "~Reset" on 560 pin 7. Testing shows that a high on pin 7 pulls the "In" on pin 6 down, via inverters in each 560 which isolate the six "In"s from one another. This sets the "+" outputs to a next counter value of 000001, and the current counter value pin 5 "~Out"s to 111111.

But it does not directly set the independent "Out"s to 000000. However pin 6 is bidirectional: pulling them down forces "Out" pin 13 of each 551 down, which clears all the output bistables, setting "~Out" on 551 pin 12 & "~In" on 560 pin 9 high, and "Out" on 560 pin 8 low.

So Reset sets the current & next values of the Microprogram Counter to 0 & 1 respectively, both during and after the pulse. On the Microprogram Counter page of CON-CIRC.PDF, arrows need to be added pointing into pin 13 of all six 551s, to show that these signals are bidirectional.

Logic LSA Summary

Having removed several LSAs from machine 5343, I've seen that most of them have a "T" number visible in their wiring layers, which usually corresponds to the last two digits of the colour coding on the edge of the LSA. For example, in LOGICSUB.PDF, the photograph of the LSA coloured 559 has "T59" at the bottom right.

However, LSA coloured 502 & 509 are marked with all three digits, "T502" & "T509". The table below sorts the LSAs in "T" number order, ignoring the leading "5" unless followed by "0", and it will be seen that no conflict arises with LSA codes starting "-" denoting an uncoloured first digit. (Colour codes "-01" to "-10" inclusive are used by the interdeck cables but do not conflict with 502 & 509).

Notch	n		
---	Dummy	---	---
551	AQJC latch	946	946 946
552	M latch	946	946 946
553	PIE latch	946	946 946
554	Adder	946	946 946
555	?		
556	Simple Carry	946	946 ---
557	Simple Carry	946	946 ---
558	LAhead Carry	930	946 946
559	LAhead Carry	946	946 930
560	Count Adder	946	946 ---
561	Decoder	930	930 ---
562	4*2Nand	cap	946 ---
563	4*2+Mixed	932	930 ---
564	2*4Nand	---	930 ---
565	2*4Buffer	---	932 ---
566	Expander	933	933 ---
567	6*Gates	930	946 cap
573	2*TxFSame	xxx	xxx 946
-74	Old -84?		
-75	Wide Latches	not	visible
-76	Wide Phases	not	visible
-77	Regulator	xxx	xxx xxx
-78	6*10Kohm		
-79	6*150ohm		
-80	Reader link		
-81	Reader link		
-82	Reader link?		
-83	Reader link?		
-84	Wide Reset&co	not	visible
585	2*RxDiff	930	xxx 933
587	2*RxFSame	930	xxx 933
502	4*2Buffer	cap	932 932
504	Reset&co	946	xxx 932
509	Init Inst	---	930 946
Notch		n	

The rightmost columns above shows which chips are used, where cap = a capacitor and xxx = various components.

My chip speculations in LOGICSUB.PDF are all correct except for LSA type 509 which I suggested was 2*930 but is actually 930+946.

*** EOF ***