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Roadmaps and Technology Reality (HDD, TAPE, NAND Flash, Optical)

Roadmaps and Technology Reality – HDD, TAPE, NAND Flash

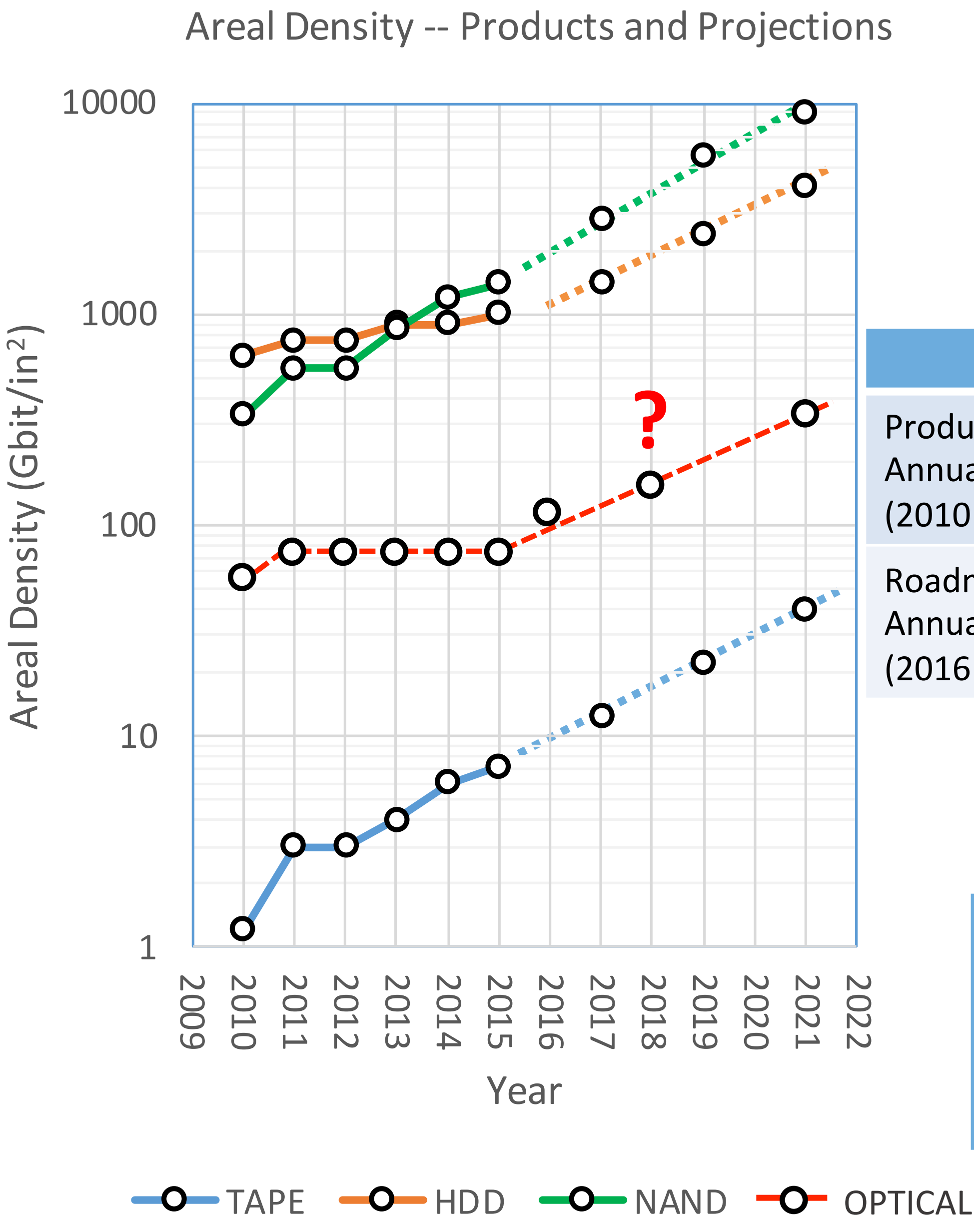
- Storage Technology Roadmaps and Figures of Merit
- 2015 Storage Landscape
- Tape Roadmap and Technology Strategy
- HDD Roadmap and Technology Strategy
- NAND Flash Roadmap and Technology Strategy
- Volumetric Density vs Areal Density
- Summary

- Key Points
  - HDD areal density slowing – Capacity achieved with more platters per drive
  - TAPE areal density continues growing at 30% per year using evolutionary technology
  - NAND Flash moving to novel process intensive 3D cell structures to sustain density growth of 40% per year

Roadmaps and Technology Reality – HDD, TAPE, NAND Flash

- Data retention and data protection clients value two "figures of merit" for storage technology components
  - Annual capacity increase
  - Annual cost per bit reduction
- The Moore's Law "contract" has been that a 2.0X capacity increase every two years (i.e. 40% per year growth) with no increase in manufacturing costs will result in a 0.5X cost per bit reduction every two years (i.e. 30% per year decrease).
- Technologists implement the Moore's Law contract for capacity and cost with "roadmaps" which predict improvements in bit density at the substrate level – areal density
- Technologists address the cost per bit part of the Moore's Law contract by emphasizing areal density strategies over volumetric density strategies
- TAPE and NAND are emphasizing areal density strategies while HDD, to compensate for nano-technology physics issues, is emphasizing volumetric strategies. The net result is that $/GB for HDD are not reducing at 30% rates.

Areal Density – More Reality



	TAPE	HDD	NAND
Product Areal Density Annual Increase (2010 to 2015)	33%/YR	10%/YR	40%/YR
Roadmap Areal Density Annual Increase (2016 to 2022)	33%/YR	30%/YR	40%/YR

HDD anticipates a technology enabler, i.e. heat assisted magnetic recording, to provide a "step" increase in density growth

Bit Cells in 2015 – HDD, TAPE, NAND Flash

- Bits shown at scale

NAND moves from 19 nm to 16 nm lithography and from 2 bit per cell (MLC) to 3 bit per cell (TLC) for planar cell designs with issues of adjacent cell interference and lower endurance designs. Strategy is to transition to larger cells with vertical (3d) stacking

NAND - TLC
1600 Gbit/in²
19nm x 19nm

NAND - MLC
1120 Gbit/in²
24nm x 24nm

HDD issues with the stability of writing small magnetic grains requires either novel thermal writing (HAMR) or aggressive use of shingled recording (SMR). The latter changes the processes for over-writing existing data.

HDD
1100 Gbit/in²
55nm x 11nm

Tape's successful migration to 10 TB cartridges with large bit cells relative to HDD and NAND suggests there is room for growth

TAPE
7 Gbit/in²
2000nm x 47nm

Technology Trends – HDD, TAPE, NAND Flash

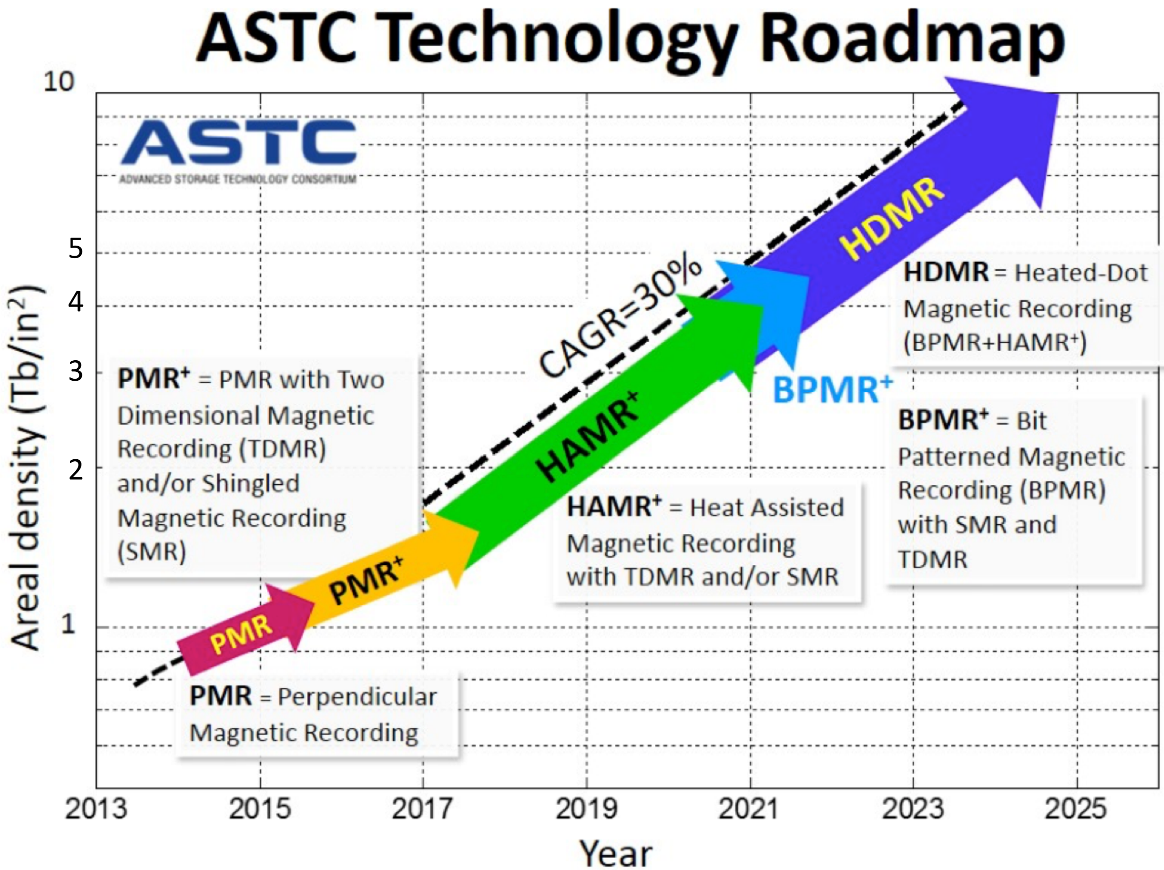
	YE 2008	YE2009	YE2010	YE2011	YE2012[1]	YE2013[2]	YE2014[3]
HDD							
Units (HDDs millions)	540	557	652	620	577	551	564
PB Shipped (PB)	125000	200000	330000	335000	380000	470000	549000
Areal Density (Gb/in²)	380	530	635	750	750	750(900)	900
Revenue ($ billions)	34.0	34.0	33.0	33.5	37.5	33.4	33.4
$/GB Shipped	0.272	0.170	0.100	0.100	0.100	0.071	0.061
NAND							
Units (2GBs millions)	1500	2715	5232	9326	14000	19500	312500
PB Shipped (PB)	3000	5430	10464	18600	28000	39000	62500
Areal Density (Gb/in²)	200	280	330	550	550	850	1200[3]
Revenue ($ billions)	10.0	12.1	18.5	21.5	22.0	24.0	32.2
$/GB Shipped	3.33	2.23	1.77	1.16	0.78	0.615	0.515
LTO TAPE							
Units (Cart. millions)	20	24	25	25	22.7	20.4	19.6
PB Shipped (PB)	10400	12165	15300	17800	19500	22500	26160
Areal Density (Gb/in²)	0.9	0.9	1.2	1.2	1.2(2.1)	2.1	2.1
Revenue ($ billions)	1.0	0.7	0.7	0.7	0.62	0.54	0.50
$/GB Shipped	0.093	0.061	0.046	0.038	0.032	0.024	0.0192

1. LTO6 introduced December 2012
2. HDD Shingle Magnetic Recording introduced late 2013
3. NAND technology moves to TLC (3 bit/cell) designs

HDD Roadmap

- ASTC* roadmap shows 2015 - 2017 areal density increase is ~ 1.4X or 18% per year. Afterwards, revolutionary technologies are needed

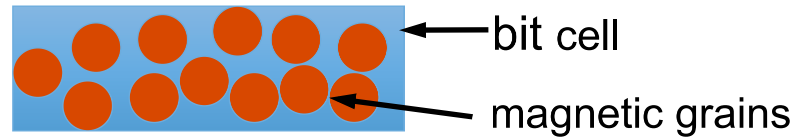
- **Smaller bit cells are thermally unstable**
- **Smaller bit cells have fewer grains**
- **Smaller bit cells require improved sensors**



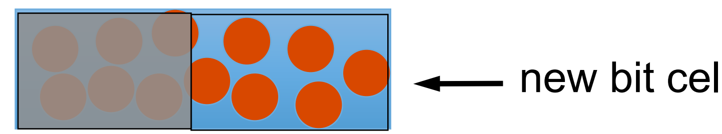
* Operating within the existing IDEMA framework, ASTC is a forum for collaborative joint R&D efforts among storage industry participants, customers, suppliers, universities and laboratories with a goal to shorten the time from invention to productization.

One of the 'Brick Wall(s)': Magnetic Storage 'Trilemma'

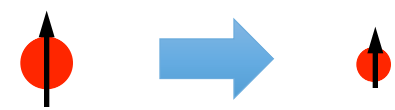
For magnetic storage to grow, the 'bit cells' that hold the 1's and 0's must shrink



But simply shrinking the bit cell would mean fewer magnetic particles (tape) or grains (disk) per cell - and fewer grains in a bit results in degraded signal-to-noise ratio (SNR). however...SNR is needed for reliable operation



No problem...just shrink the grain size and increase the number of grains in a bit cell?



Not quite...physics rules!

If the grains are too small, they will not hold onto their magnetization (flip). Thermal vibrational energy in the lattice, kT, competes with the magnetic energy of the grain, KuV (V is grain volume and Ku is magnetic volume energy density

Trilemma (conclusion)

- Some magnetic physics

  - Stable grains require that $K_u V > 60\ kT$

    Physics rules again!!!

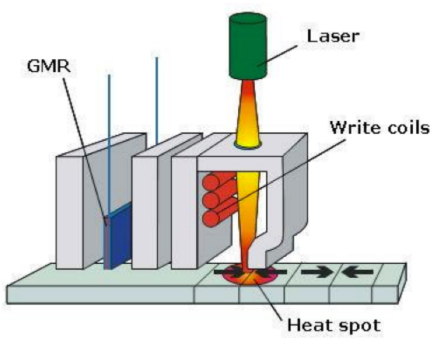
  - Increasing K_u (not trivial) makes the grains harder to magnetize, i.e. the write head must be able to provide sufficient magnetic field to magnetize the bits

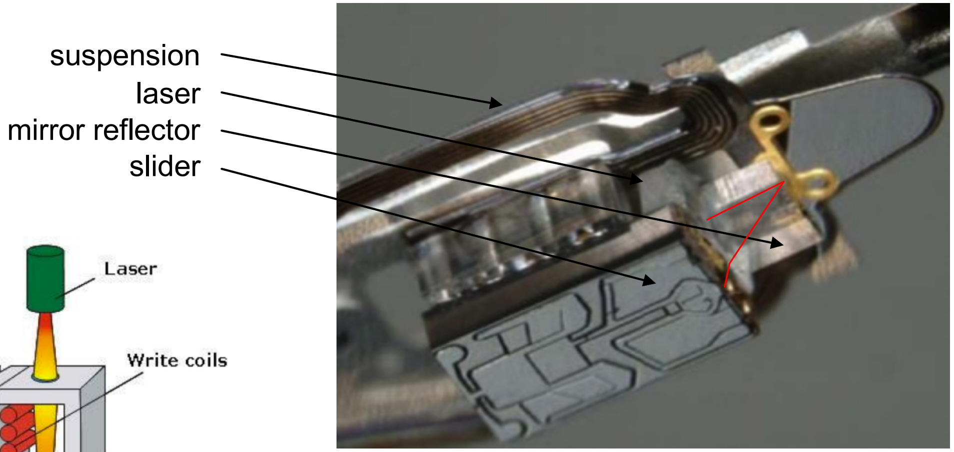
  - But magnetic field from write heads is limited by M_s of available write head materials and is not large enough for high K_u disk material

    So

  - Use heat to locally reduce the K_u during the write process with a localized heat spot from a laser excited radiator. THIS IS HAMR or Heat Assisted Magnetic Recording (HAMR)

- HAMR manufacturability requires new (and complex) recording components
  - Laser on each slider/suspension
  - Heater embedded into the head structure
  - New disk media
  - Overcoat protection for media and heater transducer for thermal cycle reliability
- Reliability and cost are issues
- Scaling has not been demonstrated to higher densities
- HAMR achieving 30% per year annual density growth can be questioned





M. Re, "Has HAMR reached a critical mass", The Information Storage Industry Consortium Symposium on Alternative Storage Technologies, April 2009, www.insic.org

The slider is about the size of a large grain of sand

NAND Areal Density

NAND has three strategies for increasing bits per unit area in a silicon chip

1 Lithographic scaling of the bit cell (x, y) dimensions by reducing F*

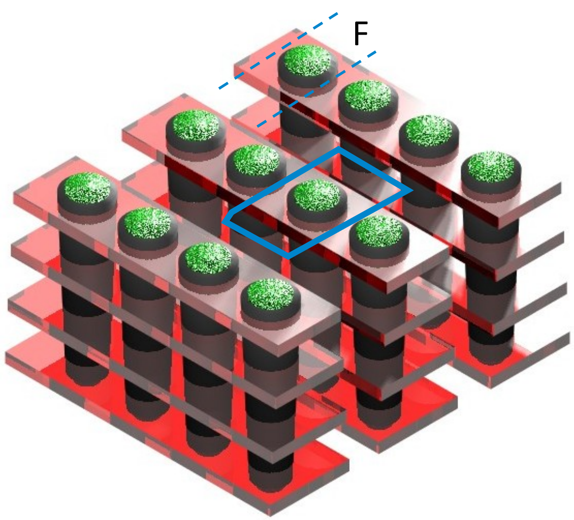
- 20nm to 16nm → 1.56X more density — Yes, 128 Gb chips today
- 16nm to 13nm → 1.51X more density — No, Inter-cell interference, insufficient charge

2 Increasing the number of bits per cell

- 1 bit per cell to MLC (2 bits per cell) → 2.00x increase — Yes, 128 Gb chips today
- MLC to TLC (3 bits per cell) → 1.50x increase — Yes, 128 Gb chips today

3 3D stacking (larger bit cell but multiple layers of cells) — Yes, the future of ≥ 128 Gb chips

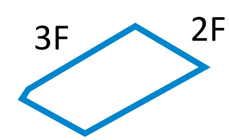
Example: 16 nm goes to 48 nm and cell design goes from $4F^2$ to $6F^2$ so cell area increases 13.5x But by using 27 layers the effective density on the surface of the wafer increases by 2.00x (27/13.5)



3D Design Example

- Basic Cell 2F x 3F (F is minimum feature)
- 12 cells per layer
- 4 layers
- 2 bits or 3 bits per cell
- 96 bits or 144 bits

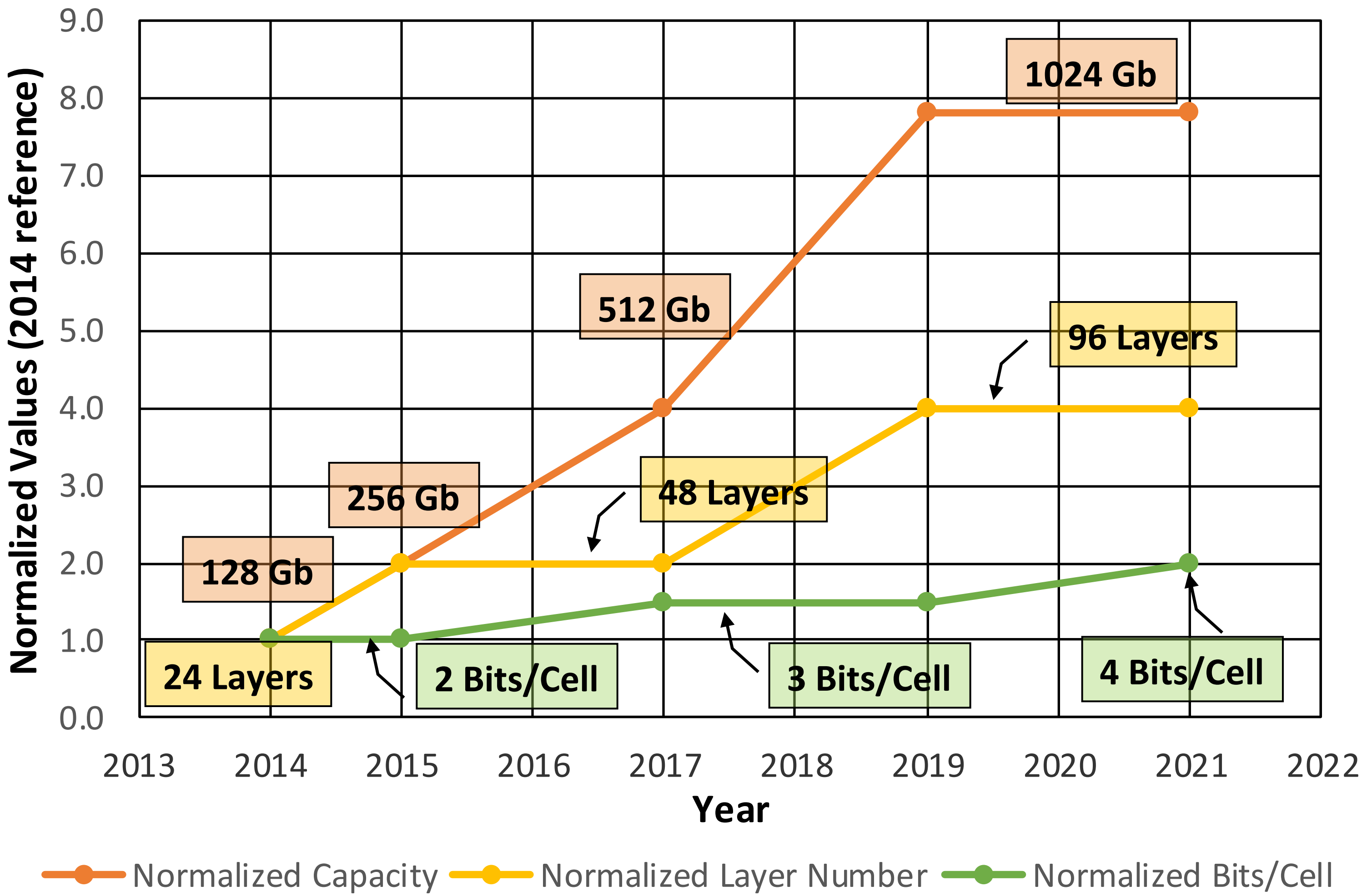
Basic Cell



*The basic NAND cell has an area of $4F^2$, where F is the minimum patterned feature forming the cell

Flash Roadmap Strategy (ITRS)

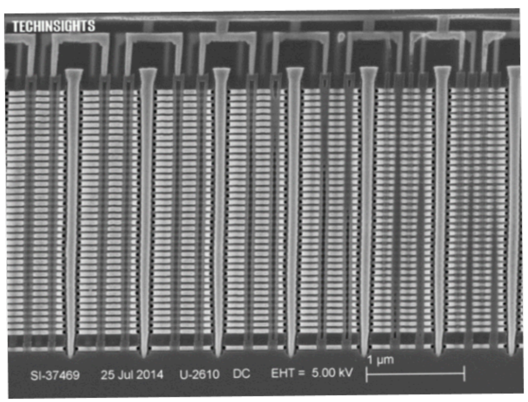
- Transition after the 16 nm node **planar cell** design to a **3D cell** design relying on increasing bits per cell by 2X and layers by 4X in a 6 year to 8 year period, i.e. 40% to 50% annual density increases



The Real NAND Issue – Scaling the number of layers by 4X

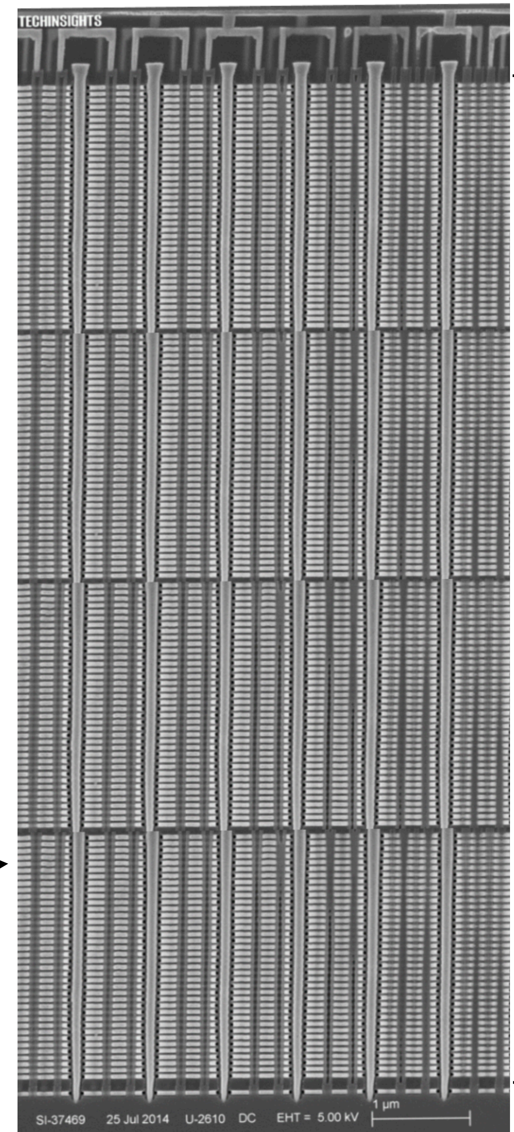
- 4X increase in layer number likely achieved only with 4 sequential process steps
- Impact is $/GB reduction

<u>TODAY (2015) 32 Layer Structure</u>
Layer Pitch ~ 67 nm
Via/Trench Opening ~ 83 nm
Trench Aspect ratio ~ 30:1!!!



2.5 um

?

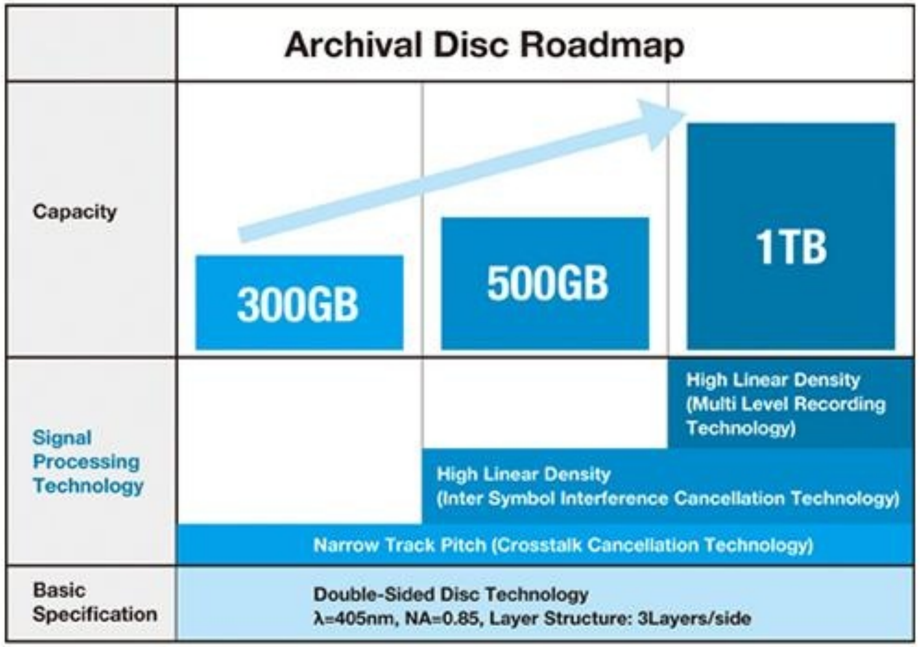


10 um

<u>TOMMOROW (2020) 128 Layer Structure</u>
Layer Pitch ~ 67 nm
Via/Trench Opening ~ 83 nm
Trench Aspect ratio ~ 120:1!!!

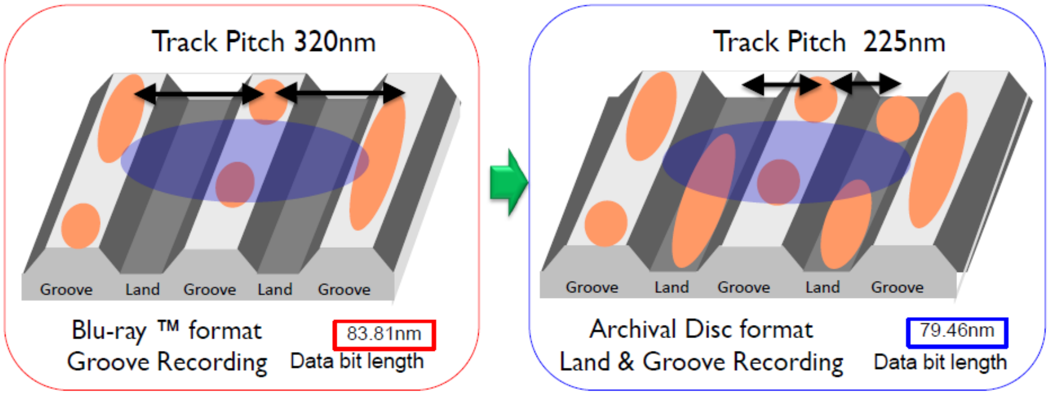
Optical Recording Roadmap (Technology with No Time Line)

- 2015 (Today): 100 GB Disk
  - 3 layers on one disk surface
  - areal density per disk surface ~ 75 $Gbit/in^2$
- 2016 (?): 200 GB Disk
  - 6 layers: 3 on top disk surface and 3 on bottom disk surface
  - Areal density per disk surface unchanged ~ 75 $Gbit/in^2$
- 201X (?): 300 GB Disk
  - **Land and groove recording to increase tracks -- PHYSICS**
  - Areal density per layer changes by 1.5X to ~ ~ 112 $Gbit/in^2$
- 202Y (?): 500 GB Disk
  - Channel algorithms to reduce bit length to increase bits along the track
  - Areal density per layer changes by 1.67X to ~ ~ 187 $Gbit/in^2$
- 202Z (?): 1000 GB Disk
  - **2 bit per cell recording by writing bits at 3 different powers -- PHYSICS**
  - Areal density per layer changes by 2.0X to ~ 375 $Gbit/in^2$

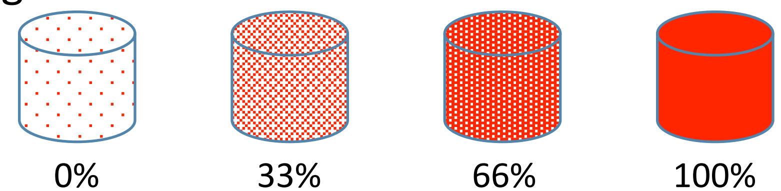


TIME (?)

- “Land and Groove” recording: Inter-track interference (reading and writing)



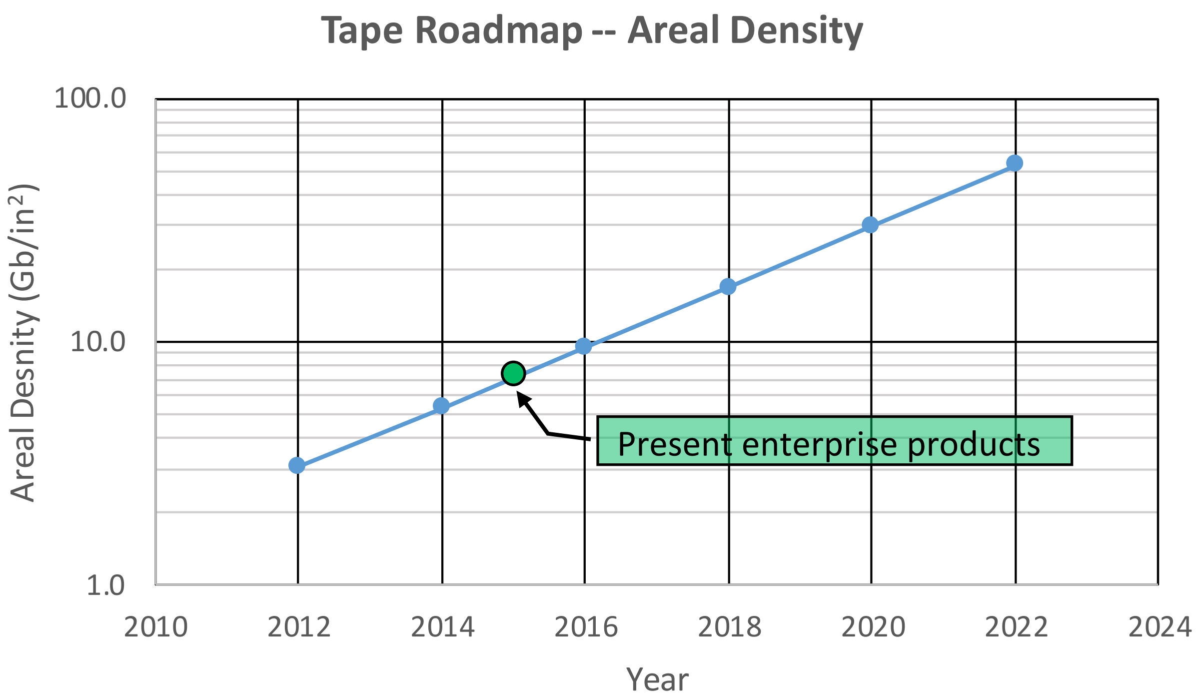
- 2 bit per cell recording: Use variable laser power to “crystalize” the phase change material into three distinct structures with reproducible reflectivity



- **Issue:** Historical annual areal density increase for optical recording ~ 12%/year so the combination of land and groove recording and 2 bit per cell recording represents a 3X increase; adding channel invention represents a 5X increase. What are reasonable expectations for density increases from history?
  - 3X increase implies 24%/yr for 5 years, 16%/yr for 7 years, 12%/yr for 9 years
  - 5X increase implies 38%/yr for 5 years, 25%/yr for 7 years, 20%/yr for 9 years

Tape Roadmaps

- Tape roadmaps established in 2013 by INSIC (International Storage Industrial Consortium) project 33% annual areal density increases. 2015 projections are being satisfied!!



- Why: The large bit cell!!!

Density Confidence Reflected in the Published 10 Generations LTO Roadmap

Future

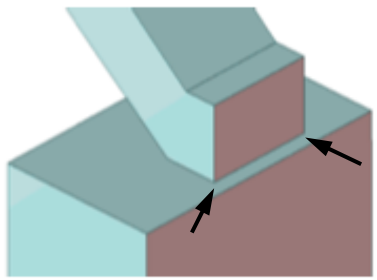
	LTO 3	LTO 4	LTO 5	LTO 6	LTO 7	LTO 8	LTO 9	LTO 10
Year	2004	2007	2010	2012	2015			
Native Capacity (TB)	0.4	0.8	1.5	2.5	6.4*	12.8	25.0	48.0
Native Data Rate (MB/s)	80	120	140	160	315*	472	708	1100
Compression Ratio	2.0	2.0	2.0	2.5	2.5	2.5	2.5	2.5
Compressed Cap (TB)	0.8	1.6	3.0	6.25	16.0	32.0	62.5	120.0
Compressed Data Rate (MB/s)	160	240	280	400	788	1180	1770	2750
*LTO7 TBD								

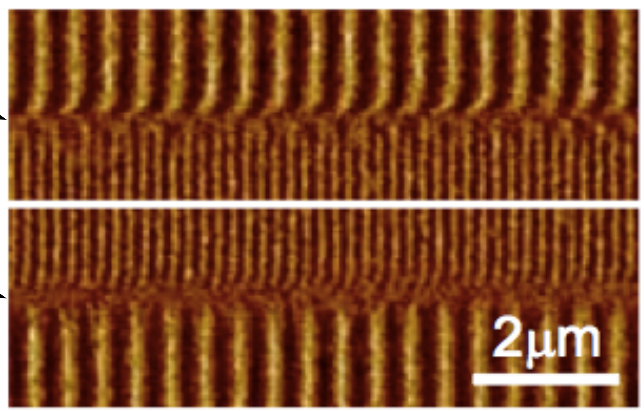
- Tape density growth is assured by the development of **<u>evolutionary</u>** technology
  - Improved track edge definition (TPI increases)
  - Improved “writeablity” of smaller size grains with high H_k (high moment heads)
  - Sensors to detect smaller bit cell widths
  - Media to support smaller bit cells

Example 1: Trimmed Writer for Better Track Edge Definition

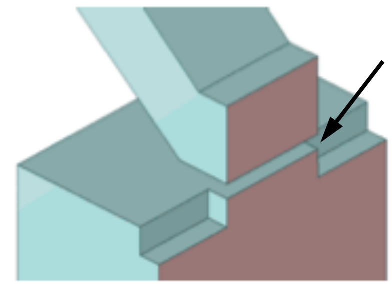
Conventional write head

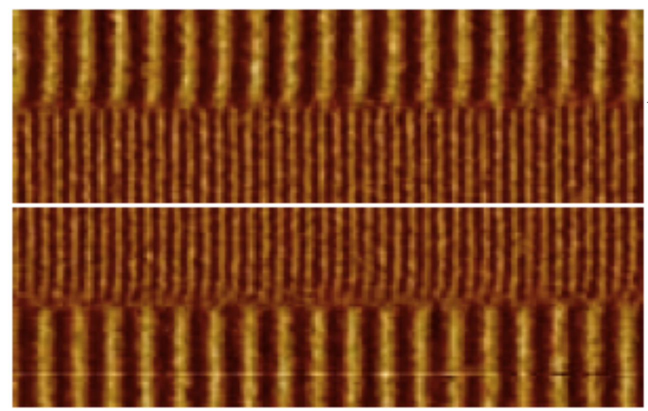
Curved transitions due to fringing fields in write heads limit achievable future track densities





Trimmed write head



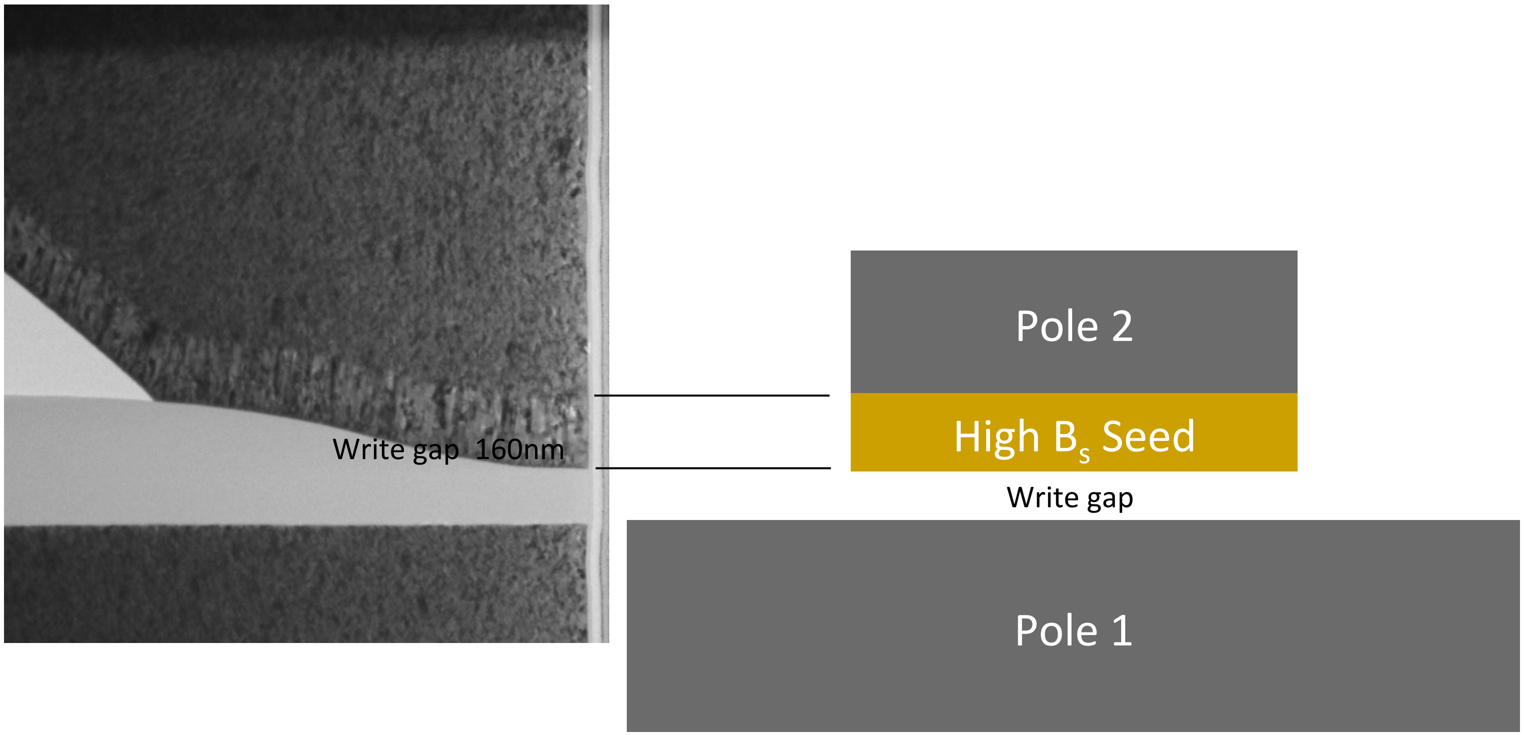


Straight transitions

Magnetic Force Microscopy of Written Tracks on Tape

Example 2: High Moment Poles

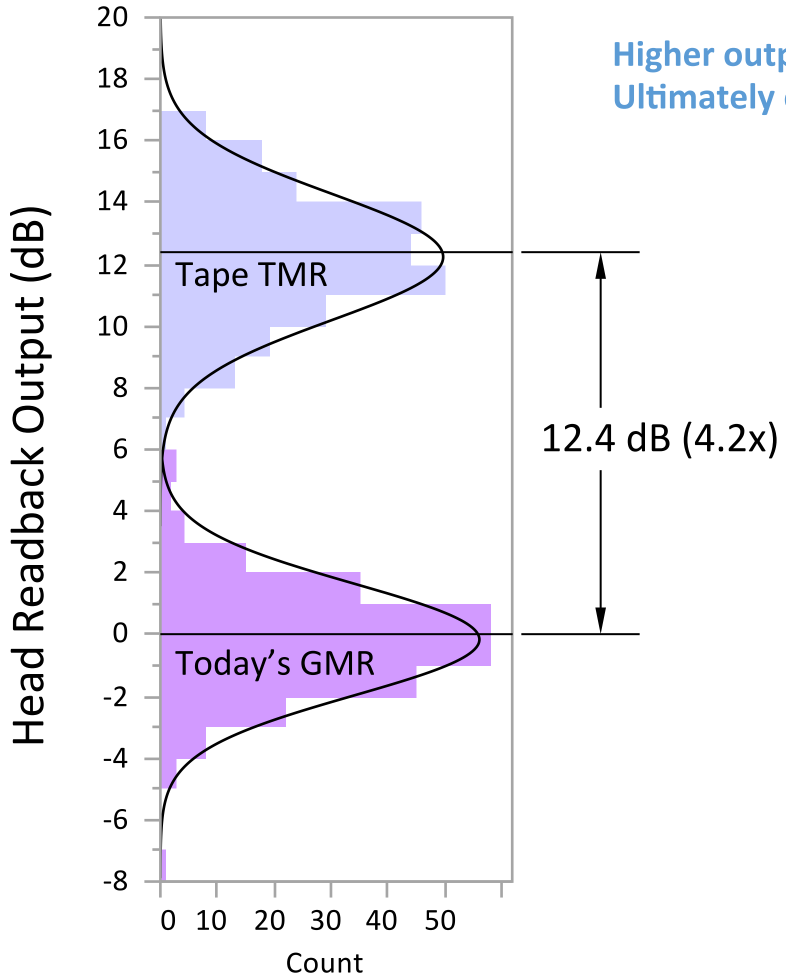
- High moment writer TEM* of IBM developed writer used in the 2015 DEMO
- Tape can increase Ku and reduce grain volume and still write with the higher moment head



*Transmission Electron Micrograph

Example 3: Tunnel Magnetoresistive (TMR) Sensor for Smaller Bit Cell Detection

- TMR* gives >4x more signal than GMR when tested under similar conditions

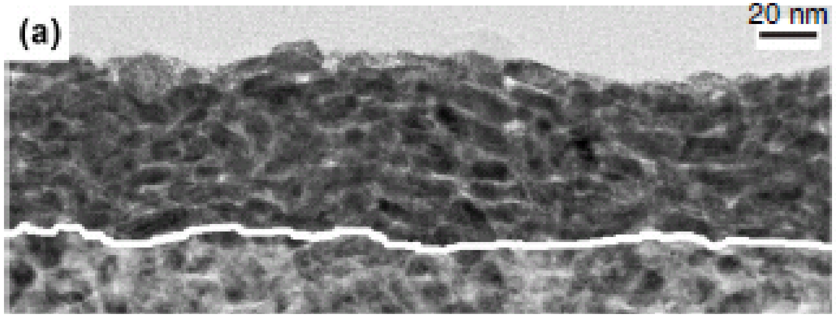


Higher output gives better reading performance
Ultimately enables growth beyond 10-15 TB cartridge

Same test platform
Same size populations
Same track width, bias
Same tape type
Similar spacing

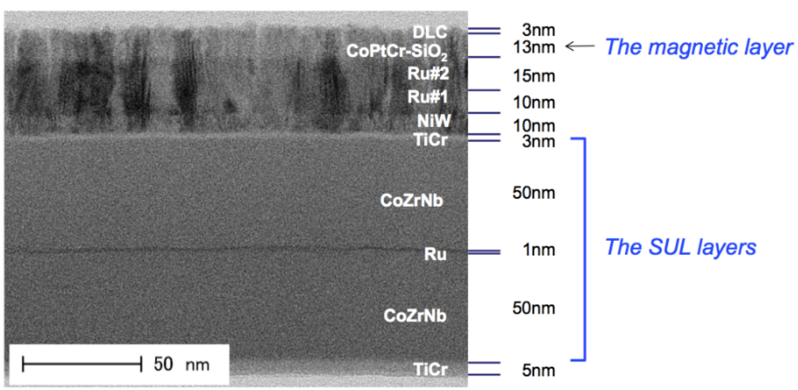
*IBM 2015 Tape Demo used an HDD TMR

Example 4: Media Development Supporting Smaller Grains



BaFe >80Gb/in^2 Particulate Media

IBM Zurich Demonstration



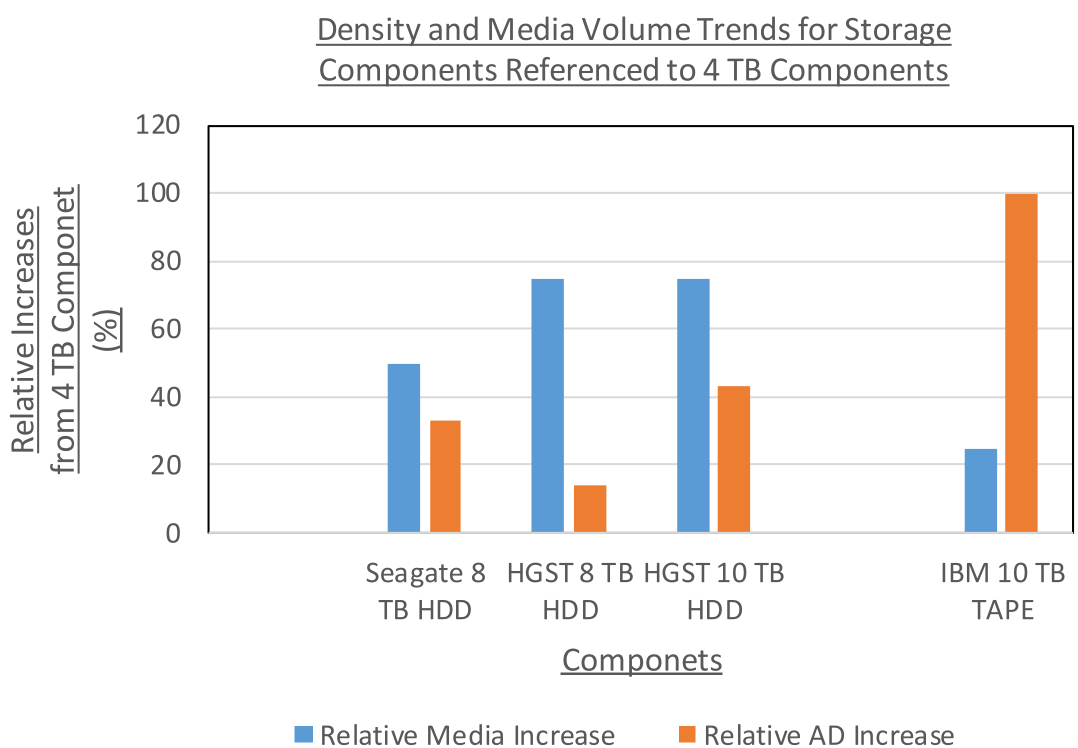
CoPtX 148Gb/in^2 Sputtered Media (i.e. like HDD Media)

IBM Zurich Demonstration

Magnetic Storage Strategies

Contrasting strategies between HDD and TAPE in transitioning to 10 TB components

- HDD - Add platters (with helium) vs increase areal density (so far via shingling)
- TAPE - Increase areal density (e.g. EDGE2015 Demo) vs thinner, longer tape



Future of NAND, Disk and Tape

- HDD areal density has been growing 20% per year, at best, over the last 3 to 4 years and is now introducing SMR. Revolutionary technology like HAMR faces extendibility (Moore's Law) challenges and is not yet proven in manufacturing.

- NAND has a near term horizon of increasing density by 2X to 3X and a long term horizon of 6X to 8X. If 8x is achieved in 6 years then this is 43% per year (aggressive), if 8 years then 30% per year. NAND areal density increases rely on transition to 3D cells and require new processing strategies with potential additive process costs as 3d layers increase. However, processing is a core expertise of the semiconductor industry so success will follow.

- Tape areal density has been growing at approximately 30% per year using evolutionary technologies and is backed up with a consistent record of demonstrations.

- Optical – Unknown time line with aggressive technology nodes

- In the next 3 years it is much more likely that tape cartridge capacity will double from 10 TB to 20 TB than 3.5" HDD disc drive capacity will double from 8 TB to 16 TB ➔ HDD has limited ability to add more platters while TAPE has a metered ~5%/yr strategy to increase tape length coupled with established areal density growth.