ES7210

High Performance Four Channels Audio ADC

FEATURES

- High performance multi-bit delta-sigma audio ADC
- 102 dB signal to noise ratio
- -85 dB THD+N
- 24-bit, 8 to 100 kHz sampling frequency
- I^2S/PCM master or slave serial data port
- Support TDM
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- Low power standby mode

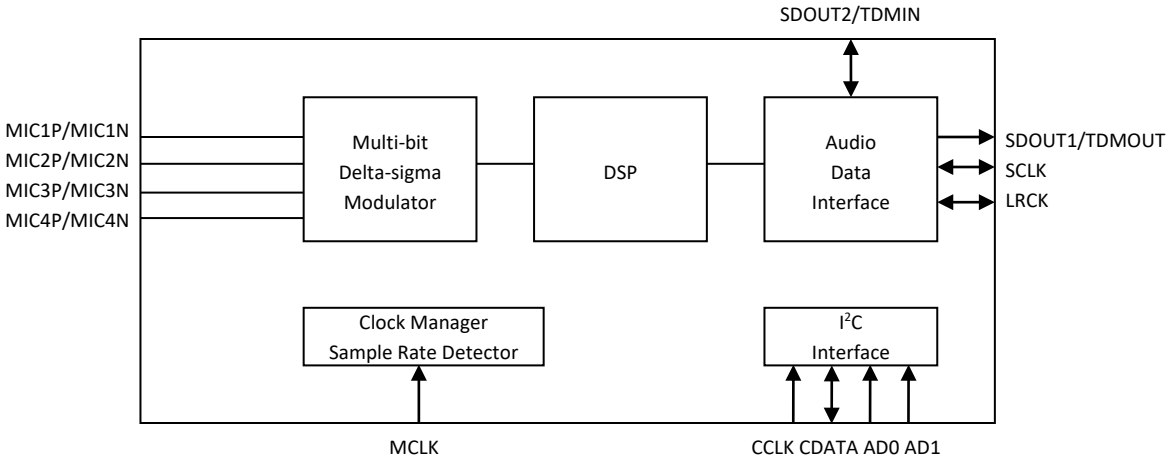
APPLICATIONS

- Mic array
- Smart speaker
- Far field voice capture

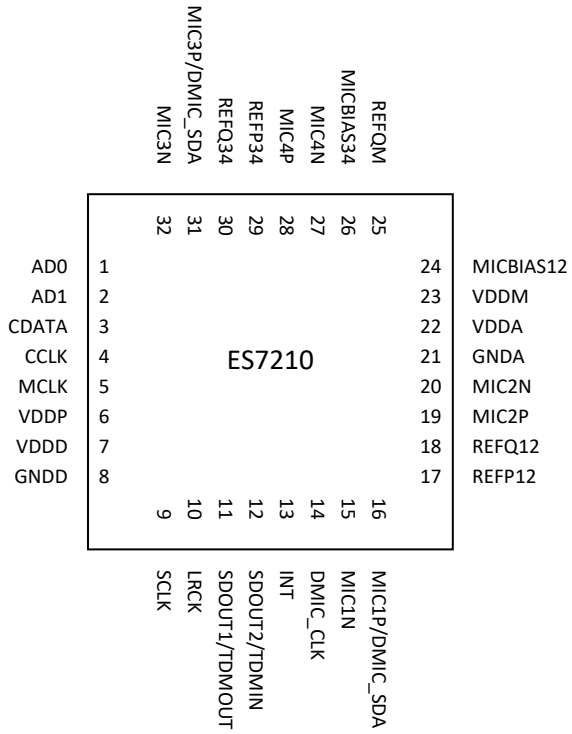
ORDERING INFORMATION

ES7210 -40°C ~ +125°C
QFN-32

BLOCK DIAGRAM

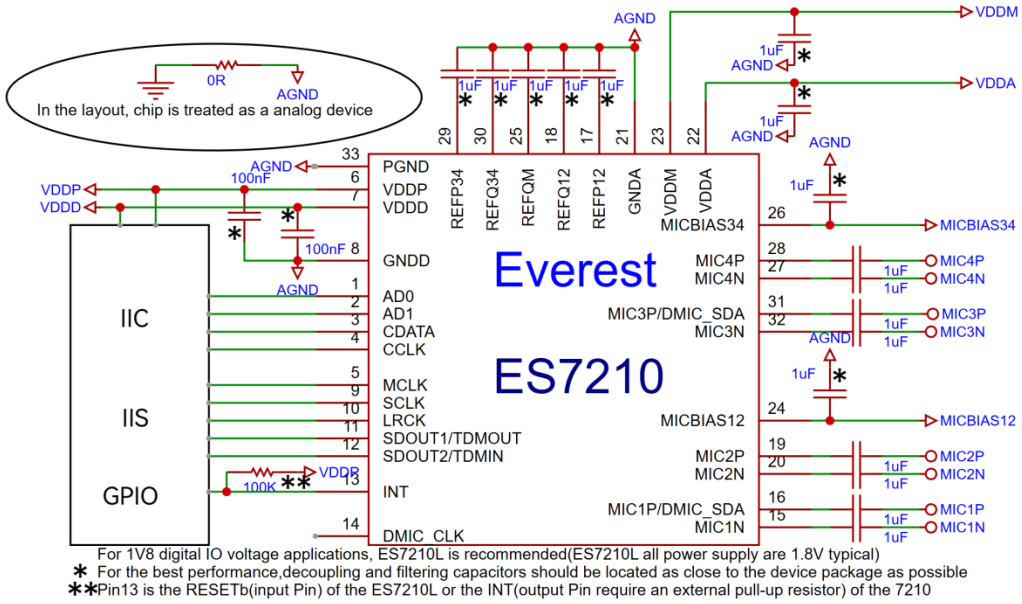


1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CDATA, CCLK	3, 4	I/O, I	I^2C clock and data
AD0, AD1	1, 2	I	I^2C address
MCLK	5	I	Master clock
SCLK	9	I/O	Serial data bit clock
LRCK	10	I/O	Serial data left and right channel frame clock
SDOUT1/TDMOUT SDOUT2/TDMIN	11 12	O I/O	Serial data output or TDM data input and output
INT	13	O	Interrupt
DMIC_CLK	14	O	Digital mic clock
MIC1P, MIC1N MIC2P, MIC2N MIC3P, MIC3N MIC4P, MIC4N	16, 15 19, 20 31, 32 28, 27	Analog	Mic input MIC1P and MIC3P can be used as digital mic data input
MICBIAS12 MICBIAS34	24 26	Analog	Mic bias
VDDP	6	Analog	Power supply for the digital input and output
VDDD, GNDD	7, 8	Analog	Digital power supply
VDDA, GNDA	22, 21	Analog	Analog power supply
VDDM	23	Analog	Analog power supply
REFP12, REFP34	17, 29	Analog	Filtering capacitor connection
REFQ12, REFQ34	18, 30	Analog	Filtering capacitor connection
REFQM	25	Analog	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT



3. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (25 MHz, 26 MHz, etc).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

4. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 1000 0x, where x equals AD1 AD0 (input pin: 1 being connected to supply and 0 being connected to ground). The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^{2}C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^{2}C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	1000 0 AD1 AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

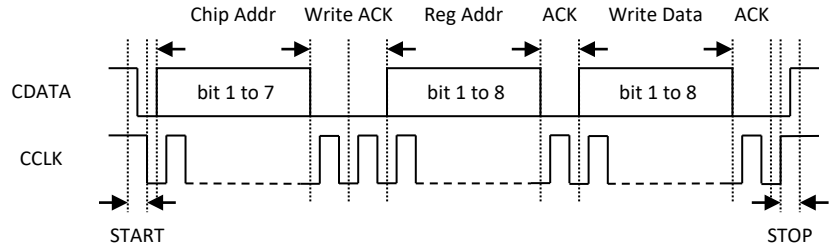


Figure 1a I^{2}C Write Timing

Table 2 Read Data from Register in I^{2}C Interface Mode

	Chip Address	R/W		Register Address		
Start	1000 0 AD1 AD0	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	1000 0 AD1 AD0	1	ACK	Data	NACK	Stop

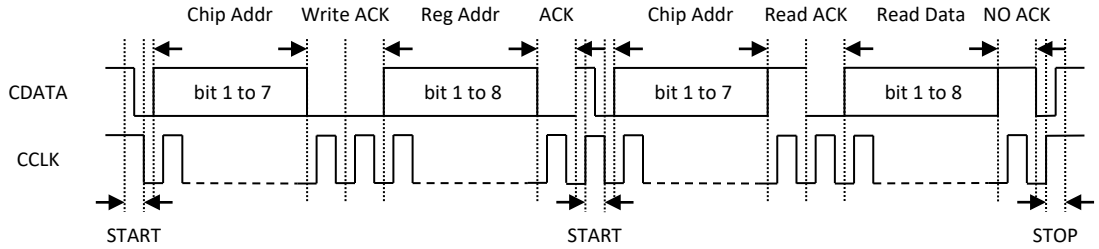


Figure 1b I^{2}C Read Timing

5. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the output from the ADC through LRCK, SCLK and SDOUT pins. These formats are I^2S, left justified, DSP/PCM mode and TDM. ADC data is out at SDOUT on the falling edge of SCLK. The relationships of SDOUT, SCLK and LRCK with these formats are shown through Figure 2a to Figure 2h. ES7210 can be cascaded up to 16-ch through single I^2S or TDM, please refer to the user guide for detail description.

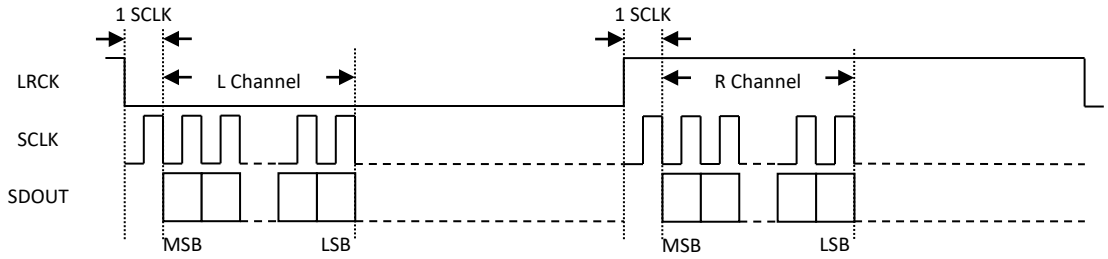


Figure 2a I^2S Serial Audio Data Format

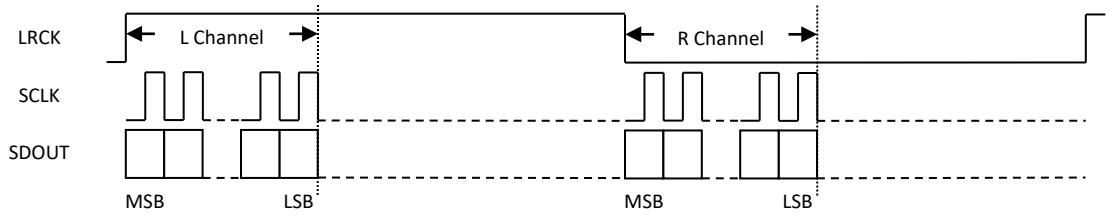


Figure 2b Left Justified Serial Audio Data Format

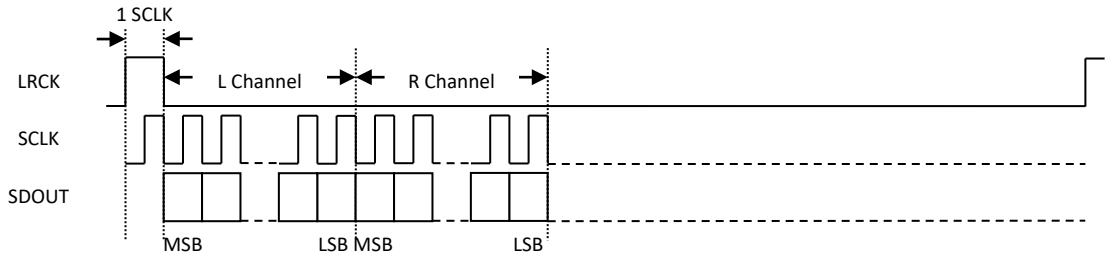


Figure 2c DSP/PCM Mode A Serial Audio Data Format

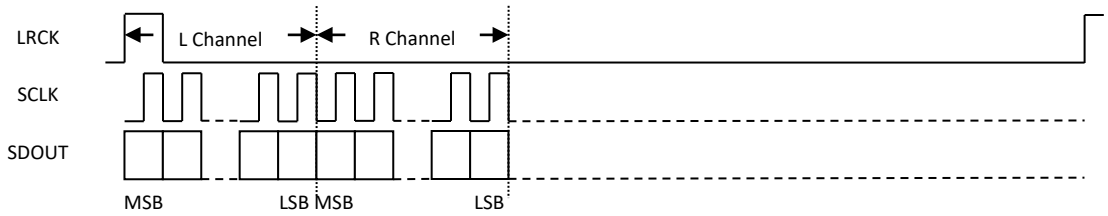


Figure 2d DSP/PCM Mode B Serial Audio Data Format

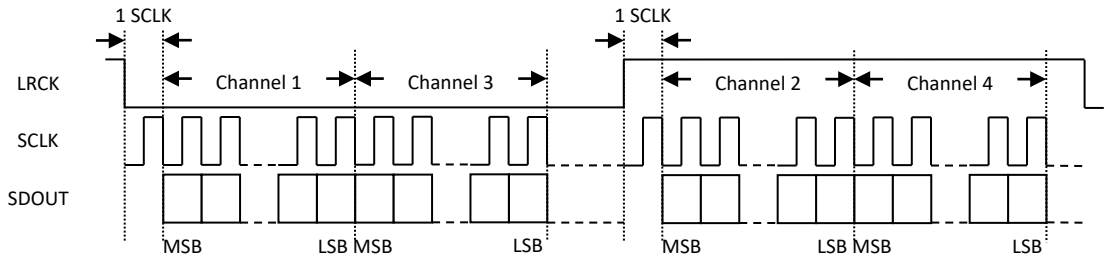


Figure 2e TDM I^{2}S Serial Audio Data Format

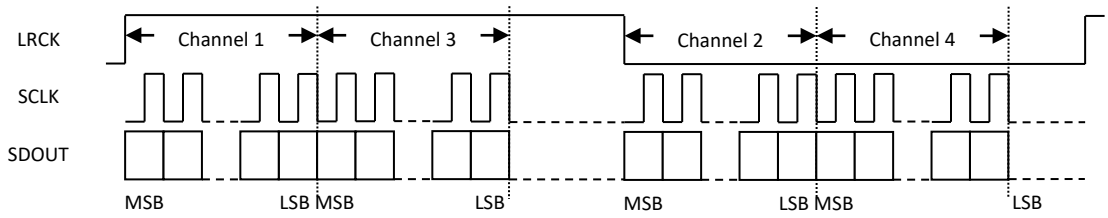


Figure 2f TDM Left Justified Serial Audio Data Format

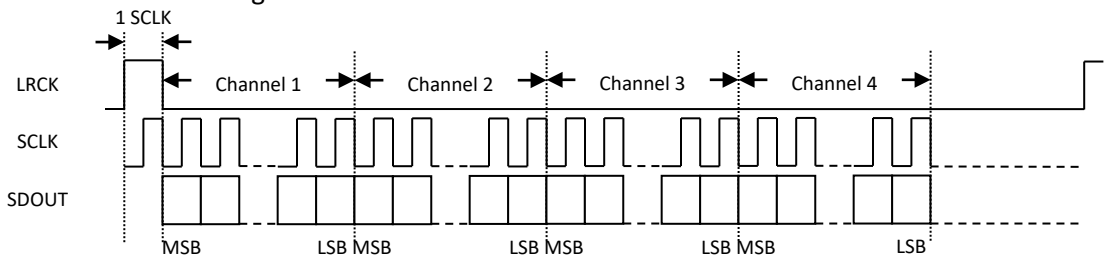


Figure 2g TDM DSP/PCM Mode A Serial Audio Data Format

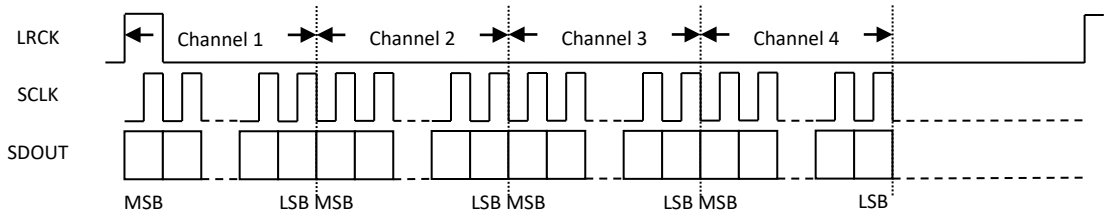


Figure 2h TDM DSP/PCM Mode B Serial Audio Data Format

6. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+3.6V
Digital Supply Voltage Level	-0.3V	+3.6V
Analog Input Voltage Range	GNDA-0.3V	VDDA+0.3V
Digital Input Voltage Range	GNDD-0.3V	VDDP+0.3V
Operating Temperature Range	-40°C	+125°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDDD	1.6	1.8/3.3	3.6	V
VDDP	1.6	1.8/3.3	3.6	V
VDDA	1.6	1.8/3.3	3.6	V
VDDM	1.6	1.8/3.3	3.6	V

Note 1: VDDD must be 3.3V (±10%), for sampling frequency higher than 1) 24 kHz in single speed 2) 48 kHz in double speed

Note 2: for VDDA less than 2V: 1) in mic application, PGA gain must be set at or above 21 dB 2) in speaker feedback application, ADC must be reset after speaker amplifier power up, if its power up transient signal is out of ADC common mode input range.

Note 3: recommend VDDP and VDDD power supply turn on or off within 10 ms of each other; VDDD must be on when VDDA is on.

Note 4: recommend all power supply on, entering low power through control register setting, then stopping input clock.

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDDA=3.3V, VDDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz or 96 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	95	102	104	dB
THD+N (-1 dB input)	-88	-85	-75	dB
Channel Separation (1KHz)	95	100	105	dB
Interchannel Gain Mismatch		0.2	1	dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs

Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input (differential P and N)		2*AVDD/3.3		Vrms
Input Impedance PGA gain 15 dB and up PGA gain 12 dB and below		6 24		KΩ

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode (Fs=16 KHz)				
VDDD=1.8V, VDDP=1.8V, VDDA=3.3V VDDD=1.8V, VDDP=1.8V, VDDA=1.8V		63 24		mW
Power Down Mode				
VDDD=1.8V, VDDP=1.8V, VDDA=3.3V VDDM=0V		10 0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*VDDP			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		VDDP		V
Output Low-level Voltage		0		V

I^2C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

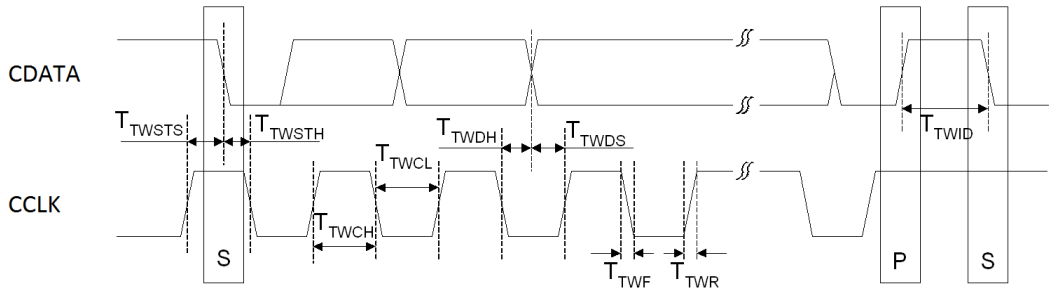


Figure 3 I²C Timing

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency (Note 5)			100	KHz
LRCK duty cycle (Note 6)		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		10	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to SDOUT valid VDDD=3.3V VDDD=1.8V	T_{SDO}		16 39	ns
LRCK edge to SDOUT valid (Note 7) VDDD=3.3V VDDD=1.8V	T_{LDO}		11 25	ns
TDMIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to TDMIN hold time	T_{SDIH}	10		ns

Note 5: up to N*100 KHz when cascaded up to 16-ch through single I²S or TDM.

Note 6: one SCLK period of high time in DSP/PCM modes.

Note 7: only apply to MSB of Left Justified or DSP/PCM mode B.

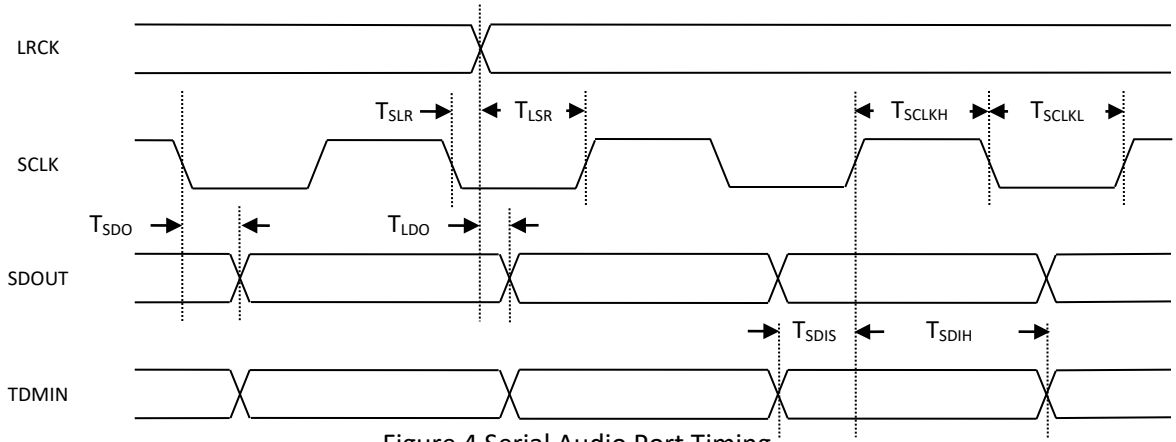
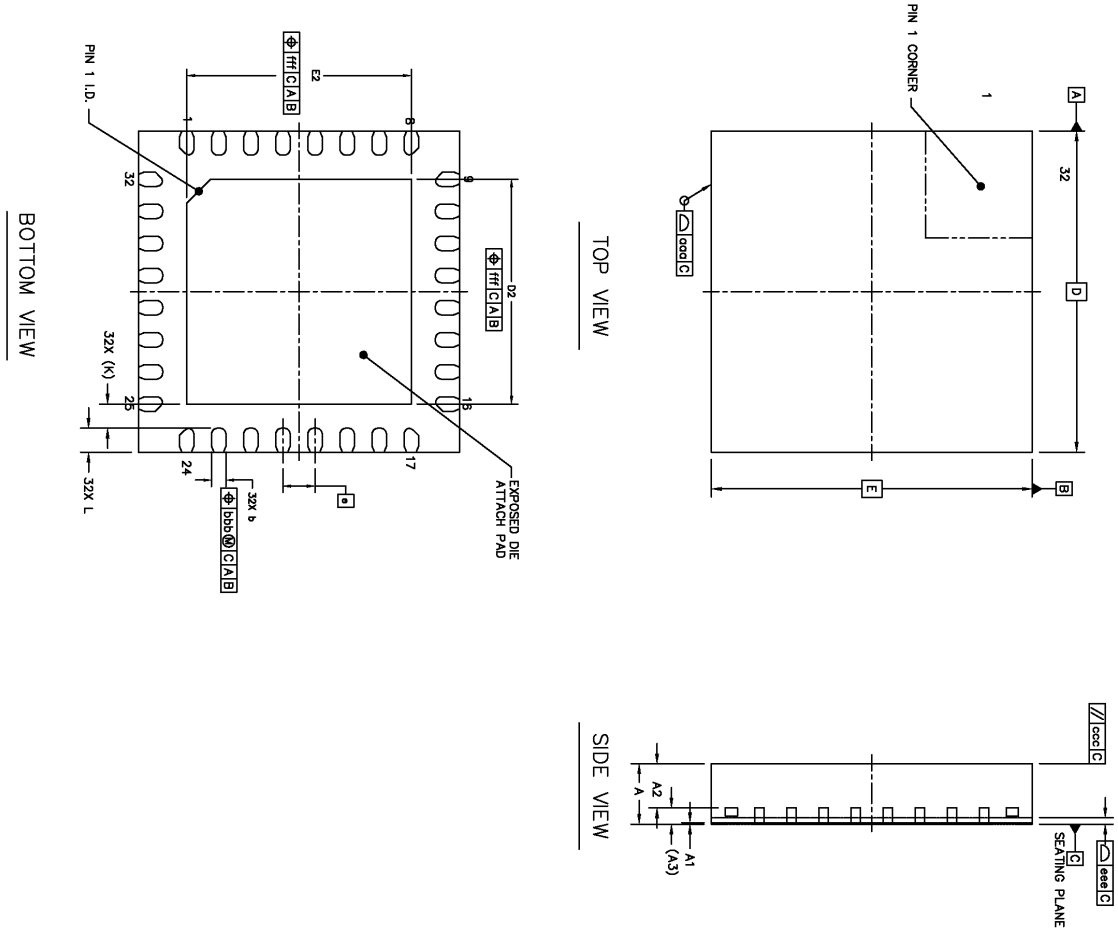


Figure 4 Serial Audio Port Timing

7. PACKAGE (UNIT: MM)



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3		0.203 REF	
LEAD WIDTH	b	0.15	0.2	0.25
BODY SIZE X	D		4 BSC	
BODY SIZE Y	E		4 BSC	
LEAD PITCH	e		0.4 BSC	
EP SIZE X	D2	2.7	2.8	2.9
EP SIZE Y	E2	2.7	2.8	2.9
LEAD LENGTH	L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE	K		0.3 REF	
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	ccc		0.1	
COPLANARITY	eee		0.08	
LEAD OFFSET	bbb		0.1	
EXPOSED PAD OFFSET	fff		0.1	

8. CORPORATE INFORMATION

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