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An Integrated System Evaluation Engine for Cross-Domain Simulation and Design Optimization of High-Speed 5G Millimeter-Wave Wireless SoCs

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Abstract

This paper develops an Integrated System Evaluation Engine (ISEE) based on Matlab, Advanced Design System (ADS), and Cadence simulators, for evaluating system performances of wireless communication transceiver (TRx) using high-order complex modulation schemes. The evaluation can be from either transistor-level, behavior model level, or even experimental results of modules that are already fabricated. To demonstrate effectiveness and efficiency of using ISEE for high-speed SoC design optimization, several 28 GHz direct-conversion TRx front-end systems are designed and simulated using orthogonal frequency division multiplex (OFDM) signals with sub-carriers modulated by quadrature amplitude modulation (M-QAM) scheme. The TRx system includes a Doherty transmitter (Tx) and three different receivers (Rx) for comparison. The co-simulation results reveal the merits and demerits of three Rx architectures and lead to design insights for Rx front-end circuits operated with advanced modulation formats.

1. Introduction

As the increasing demand for the wireless mobile data traffic continues to grow dramatically, multiple millimeter-wave (mm-wave) bands have been specified and investigated for 5G and beyond mobile networks to deliver ultra-high-speed wireless backhaul connectivity. Highly integrated mm-wave transceiver front-end has been actively studied to support the deployment of multi-Gbps data rate wireless communication systems. Furthermore, wideband modulated signals are always utilized in communication systems for improving the data rate and spectrum efficiency. Traditionally, RF and millimeter-wave (mm-wave) circuits are simulated by continuous-wave (CW) signal during design stage, while the circuits are used for dealing with modulated signals after fabrication. It results in that circuits' performance cannot be accurately predicted during design stage. Thus, it is very meaningful to construct a co-simulation platform to evaluate the performances of transceiver systems using high-order modulated signals in the design procedure.

This paper presents an Integrated System Evaluation Engine [1] to enable the simulation utilizing advanced modulation schemes. The engine is implemented using Matlab, ADS and Cadence software. To demonstrate ISEE, a 28 GHz transceiver front-end system is constructed and evaluated using orthogonal frequency division multiplex signal, whose sub-carrier consists of high order quadrature amplitude modulation signal. Three different Rx front-end circuits (Rx-1, Rx-2, and RX-3) are designed and compared for the demonstration.

2. Integrated System Evaluation Engine

The diagram of the ISEE is depicted in Fig. 1(a), mainly including two parts: signal modulation/ demodulation and circuit simulation. The modulation and demodulation of the baseband (BB) signal are completed in Matlab, while the circuit simulation is conducted in ADS, Cadence, and EMX. To utilize the co-simulation platform readily, a GUI is implemented using Matlab, as illustrated in Fig. 1(c). The left-hand side of the GUI is the parameter setting panel and the right-hand side shows the simulated and demodulated results.

The modulation process is triggered by clicking the Signal Modulation icon on the GUI. After modulation, the characteristics of the transmitted BB signal, such as the baseband spectrum and constellation of the M-QAM OFDM signal, will be displayed on the GUI. The demodulation process comes into operation after clicking the Signal Demodulation icon. Other than the spectrum and constellation, the calculated BER, EVM and data rate of the received BB signal will be shown on the GUI after demodulation, as shown in Fig. 1(c).

The architecture of the designed 28 GHz direct-conversion transceiver front-end system is shown in Fig. 1(b). The BB I/Q signals generated in the above section are up-converted to RF frequency by the I/Q mixers, and then transmitted by an emitting antenna after amplifying. An equation-based channel is used to connect the Tx and Rx [2]. Subsequently, the received signal is down-converted by I/Q mixers to BB I/Q signals. Though ADS

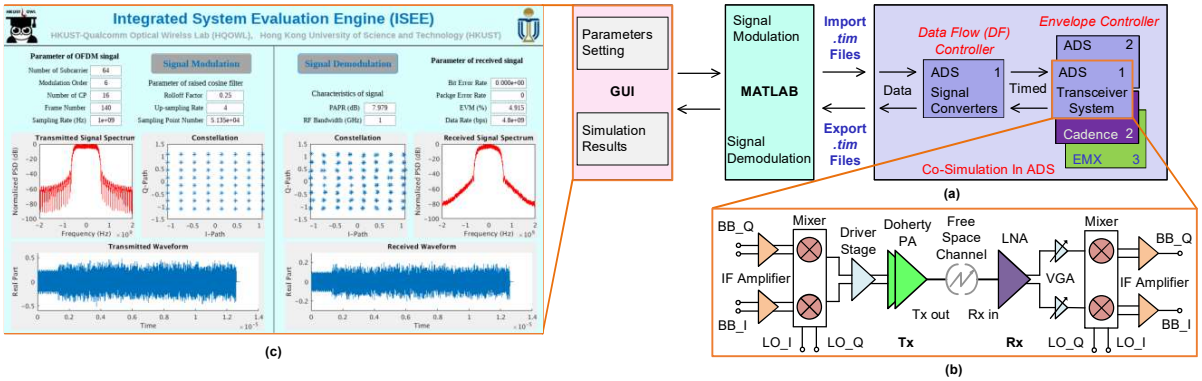


Fig. 1. (a) Diagram of ISEE. (b) Architecture of the 28 GHz TRx front-end system. (c) The graphical user interface of ISEE.

provide users with a friendly circuit design and simulation environment, Cadence is more compatible with integrated circuit design kit. Thus, if the sub-circuits of the transceiver are designed using Cadence, the connection between Matlab and Cadence can be established by either using ADS and Cadence simulators dynamic link provided by Keysight, or changing the formats of importing data from Matlab and exporting data from Cadence to be .dat and .csv, respectively.

3. 28 GHz Transceiver Front-End Circuit

This section shows the design and CW signal simulation results of the Tx and three different Rx front-end circuits.

3.1 Design and CW-Simulation of Transmitter

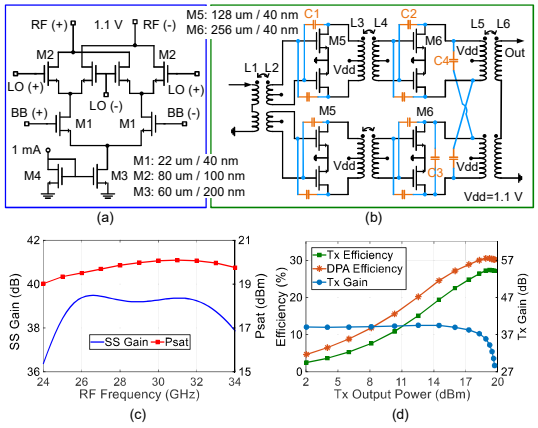


Fig. 2. Schematics of (a) the up-conversion mixer and (b) Doherty power amplifier. (c) Simulated SS gain and Psat of the Tx versus RF frequency. (d) Simulated Tx efficiency and gain versus output power.

The Tx consists of two BB amplifiers, a I/Q modulator, a driver stage, and a Doherty power amplifier (DPA), as shown in Fig. 1(b). The DPA is adopted to improve the DC-to-RF efficiency of the Tx [3]. The active double-balanced Gilbert cell shown in Fig. 2(a) is used to construct the I/Q modulator. Between the DPA and I/Q modulator, a driver stage is inserted to provide the DPA with enough input power. The schematic of the DPA is illustrated in Fig. 2(b). The parasitics of the transistor interconnections are extracted using EMX simulator, for the large transistor size used in DPA.

In the Doherty transmitter, both the carrier and peaking PAs consist of a two-stage differential PA with neutralized capacitors. A serial combining transformer with cross-connected capacitors (C4) is proposed to enhance the efficiency of the DPA. In this way, firstly, the combining transformer can be fully utilized when the peaking PA is in the off-state [3]. Secondly, the DC supply can be introduced at the center tap due to the fully symmetrical structure. Thirdly, C4 can be considered as part of the matching network.

The simulation results of the Tx front-end under the excitation of a CW signal are shown in Fig. 2(c) and (d). The simulated small signal (SS) gain and saturation output power (Psat) with respect to RF frequency are depicted in Fig. 2(c), which shows the Tx achieves a SS up-conversion gain of 38.4-39.5 dB and delivers a Psat of 19.3-20.1 dBm. At 28 GHz, the Tx delivers a Psat of 19.7 dBm and achieves a P1dB of 17.5 dBm, as shown in Fig. 2(d). The figure also indicates the Tx achieves DC-to-RF conversion efficiencies of 27.2% and 17.5% at Psat and 6-dB back-off power levels. For the DPA, the drain efficiencies are 30.2% and 22.5% at Psat and 6-dB back-off power levels, respectively. The 28 GHz Tx front-end consumes 56.6 mW from a 1.1 V supply voltage. The average output power of the Tx remains at 8 dBm when evaluating three Rx front-end systems below.

3.2 Design and CW-Simulation of Receivers

The broadband Rx-1 includes an LNA, two variable gain amplifiers (VGAs), a I/Q demodulator and two BB amplifiers (see Fig. 1(b)). Fig. 3(a) and (b) illustrate the

schematic of the LNA, the VGA and the I/Q demodulator. Same as in [4], the LNA adopts a differential gm-boosted common-gate architecture, and a compact three-coil transformer is employed to perform single-ended to differential conversion, broadband input matching, gm-boosting, and noise suppression at the LNA input. The I/Q demodulator adopts a folded architecture for wideband operation. Fig. 3(c) shows Rx-1 achieves a conversion gain of 32.8-34.7 dB, a S11 of less than -15.1 dB, and a noise figure (NF) of 2.8-3.2 dB across 25.0-32.5 GHz. Furthermore, using a two-tone simulation with a 20 MHz separation, The Rx-1 demonstrates an IIP3 of more than -20.1 dBm at 28 GHz, as shown in Fig. 3(d). The Rx-1 front-end consumes 31.5 mW from a 1 V supply voltage, as shown in Fig. 4.

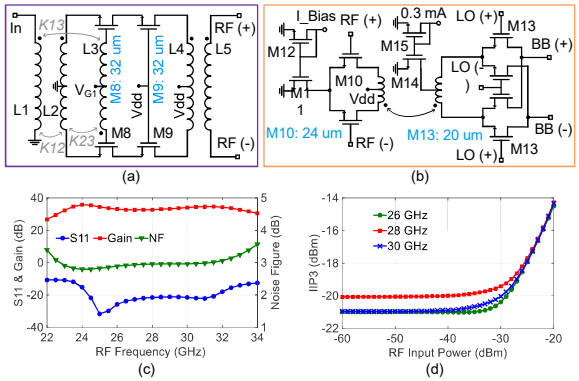
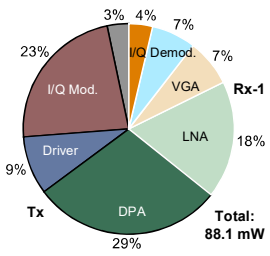


Fig. 3. Schematics of (a) LNA and (b) VGA and I/Q demodulator of Rx-1. (c) Simulated S11, voltage gain and noise figure versus RF frequency of Rx-1. (d) Simulated IIP3 of the Rx-1 with respect to RF input power.



Blocks		Voltage (V)	DC Power (mW)	
Tx	IF Amp.	1.1	2.9	56.6
	I/Q Mod.	1.1	20.2	
	Driver	1.1	7.9	
	DPA*	1.1	25.6	
Rx-1	LNA	1	15.9	31.5
	VGA	1	6.4	
	I/Q Demod.	1	6.0	
	IF Amp.	1	3.2	

Fig. 4. Power breakdown of the Tx and Rx-1.

Another two receivers (Rx-2 and Rx-3) are designed for comparison and further validation of ISEE. As shown in Fig. 5(a) and (b), Rx-2 comprises a cascode common source stage single-ended LNA with inductive degeneration [5], two passive mixers, and two BB amplifiers. The CW signal simulation results of Rx-2 show a voltage gain of larger than 31.6 dB, a S11 of less than -15.3 dB, a NF of 2.9-3.9 dB, and an IIP3 of larger than -17 dBm over 26.5-31.5 GHz. Fig. 5(c) and (d) show the block diagram and schematic of the Rx-3, which consists of a LNA, two active mixers and two BB amplifiers. The architecture of the LNA in Rx-3 is the same as that in Rx-2 and thus not given in Fig. 4(d). The Rx-3 achieves a voltage gain of larger than 30.7 dB, a S11 of less than -11.2 dB, a NF of less than 3.2 dB, and an IIP3 of larger than -18.3 dBm over 27-29 GHz.

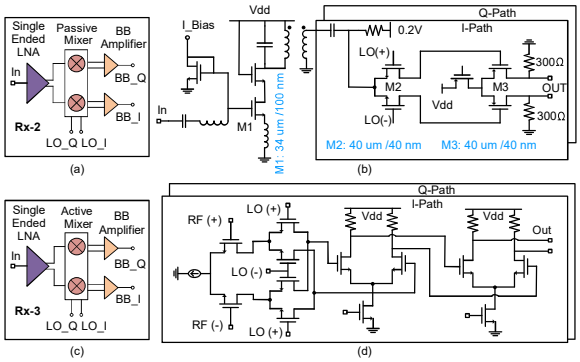


Fig. 5. (a) Block diagram and (b) schematic of Rx-2. (c) Block diagram and (d) schematic of Rx-3.

4. Cross-Domain Simulation Utilizing ISEE

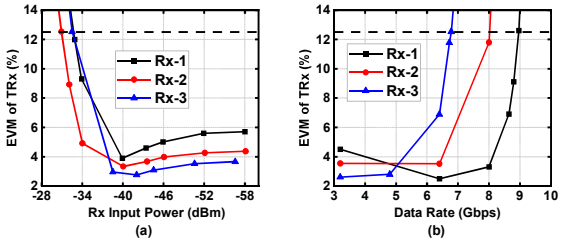


Fig. 6. Simulated EVM of the 16-QAM OFDM signal versus (a) Rx input power and (b) data rate.

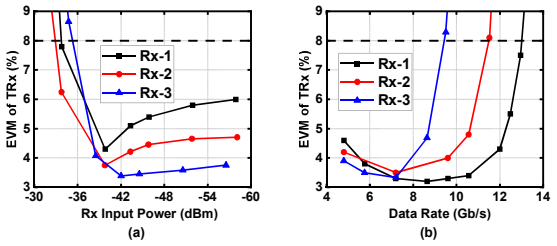


Fig. 7. Simulated EVM of the 64-QAM OFDM signal versus (a) Rx input power and (b) data rate.

Using ISEE, the three Rx front-end systems are then simulated by a 16-QAM OFDM signal with a peak-to-average ratio (PAPR) of 7.6 dB. The Tx front-end circuits used in three simulations are the same. Fig. 6(a) shows the received signal EVM versus Rx input power when the bandwidth of the OFDM signal is 1 GHz. The simulation results indicates that all the three TRx systems achieve best system EVM when the Rx input power is around -40

Table 1 Performance comparison table of three Rx front-end circuits.

Parameters		Rx-1	Rx-2	Rx-3
NF (dB)		2.8 – 3.1	3.0 – 3.2	2.9 – 3.9
Bandwidth (GHz)		25.0 – 32.5	26.5 – 31.5	27.0 – 29.0
Voltage Gain (dB)		32.8 – 34.7	28.9 – 31.3	31.6 – 34.5
IIP3 (dBm)		-22.3 – -19.4	-18.6 – -16.5	-20.8 – -17.6
S11 (dB)		< -15.1	< -10.1	< -15.3
Pdc (mW)		31.5	16.8	18.3
64-QAM Simulation with the Same TX	Number of Subcarrier	64	64	64
	Pavg (dBm)	-41.7	-41.9	-40.4
	Signal BW [GHz]	2.7	2.4	2
	Data Rate (Gbps) @ EVM (%)	13.1	11.5	9.5
		8.0	8.1	8.0
FoM* (bps/Hz)		2.0	4.8	4.0
$* FoM = \frac{Gain \times IIP3[mW] \times Data\ Rate[bps]}{Pdc[mW] \times (F-1) \times EVM \times Signal\ BW[Hz]}$				

dBm. The simulated EVM versus data rate curves of three TRx systems are shown in Fig. 6(b) when the Rx input power is around -41.8 dBm. Considering 12.5% EVM requirement for the 16-QAM OFDM signals [6], 9.0, 8.0 and 6.7 Gbps data rate can be achieved by the TRx systems with Rx-1, Rx-2, and Rx-3, respectively.

Further, the TRx front-end systems are evaluated by a 64-QAM OFDM signal with a PAPR of 8 dB. The simulated EVM of the three TRx systems versus Rx input power is shown in Fig. 7(a). Similar with the 16-QAM OFDM signal simulation results, three TRx systems achieve the best system EVM when the Rx input power is around -40 dBm. The simulated EVM versus data rate of 64-QAM OFDM signal curves are shown in Fig. 7(b).

Table 1 shows the performance comparison between three Rx front-end circuits. Considering 8% EVM requirement for 64-QAM OFDM signals [6], TRx with Rx-1 supports the highest data rate of 13.1 Gbps and Rx-3 supports the lowest data rate of 9.5 Gbps. And TRx with Rx-2 receives the highest FoM mainly due to the low power consumption of the passive mixers.

5. Conclusion

Considering the expensive IC fabrication cost, an Integrated System Evaluation Engine for evaluating high-speed system with complex modulated signals is implemented in this paper. A 28 GHz TRx system with three different Rxs is designed and evaluated by ISEE. The demonstration shows that ISEE can enhance the effectiveness and efficiency of designing and optimizing high-speed SoC significantly.

Generally, ISEE is engineered to help IC designer to evaluate their circuits at system level using practical modulated signals before fabrication, improving the success rate of chip design. And it can also help IC designers to compare and choose system architecture, saving design cost and time. In the future, ISEE can be further developed as an engine for complex system synthesis with known circuit templates.

Acknowledgments

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