ESP32 Chip Revision v3.0

User Guide

Version 1.3
Espressif Systems

About This Guide

This document describes differences between chip revision v3.0 and previous ESP32 chip revisions.

Release Notes

Date	Version	Release notes
2020.01	V1.0	Initial release.
2020.07	V1.1	Added item 6 to Chapter 1 Design Changes in ECO V3.
2022.10	v1.2	Replaced “ECO” with “Chip Revision” Renamed this document as “ESP32 Chip Revision v3.0 User Guide”
2022.11	v1.3	Added item 1 to Chapter 1 Design Changes in ECO V3.

Documentation Change Notification

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1. Design Changes in Chip Revision v3.0

Espressif has released ESP32 chip revision v3.0 that features wafer-level changes basing on previous ESP32 chip revisions. The design changes introduced on the ESP32 chip revision v3.0 are:

1. Fixed "Due to the flash start-up time, a spurious watchdog reset occurs when ESP32 is powered up or wakes up from Deep-sleep". Details of the issue can be found in item 3.8 in *ESP32 Series SoC Errata*.
2. PSRAM Cache Bug Fix: Fixed “When the CPU accesses the external SRAM in a certain sequence, read & write errors can occur”. Details of the issue can be found in item 3.9 in *ESP32 Series SoC Errata*.
3. Fixed “When each CPU reads certain different address spaces simultaneously, a read error can occur”. Details of the issue can be found in item 3.10 in *ESP32 Series SoC Errata*.
4. Optimized 32.768 KHz crystal oscillator stability. The issue was reported by client that there is a low probability that on chip revision v1.0 hardware, the 32.768 KHz crystal oscillator couldn’t start properly.
5. Fixed Fault injection issues regarding secure boot and flash encryption are fixed. Reference: *Security Advisory concerning fault injection and eFuse protections (CVE-2019-17391)* & *Espressif Security Advisory Concerning Fault Injection and Secure Boot (CVE-2019-15894)*
6. Improvement: Changed the minimum baud rate supported by the TWAI module from 25 kHz to 12.5 kHz.
7. Allowed Download Boot mode to be permanently disabled by programming new eFuse bit UART_DOWNLOAD_DIS. When this bit is programmed to 1, Download Boot mode cannot be used and booting will fail if the strapping pins are set for this mode. Software programs this bit by writing to bit 27 of EFUSE_BLK0_WDATA0_REG, and reads this bit by reading bit 27 of EFUSE_BLK0_RDATA0_REG. Write disable for this bit is shared with write disable for the flash_crypt_cnt eFuse field.

2. Impact on Customer Projects

This section is intended to help our customers to understand the impact of using chip revision v3.0 in a new design or replacing older version SoC with chip revision v3.0 in existing design.

2.1. Use Case 1: Hardware and Software Upgrade

This is the use-case where the new project is being initiated or upgrade for hardware and software in an existing project is a possible option. In such a case, the project can benefit from protection against fault injection attack and can also take advantage of newer secure boot mechanism and PSRAM cache bug fix with slightly enhanced PSRAM performance.

1. Hardware Design Changes:

   Please follow the latest *ESP32 Hardware Design Guidelines*. For 32.768 KHz crystal oscillator stability issue optimization, please refer to Section *Crystal Oscillator* for more information.

2. Software Design Changes:

   1) Select **Minimum configuration** to **Rev3**: Go to ***menuconfig*** > ***Conponent config*** > ***ESP32-specific***, and set the ***Minimum Supported ESP32 Revision option*** to "***Rev 3***".

   2) **Software version**: Recommend to use RSA-based secure boot from ESP-IDF v4.1 and later. ESP-IDF v3.X Release version can also work with application with original secure boot V1.

2.2. Use Case 2: Hardware Upgrade Only

This is the use-case where customers have existing project which can allow hardware upgrade but software needs to remain the same across hardware revisions. In this case the project gets benefit of security to fault injection attacks, PSRAM cache bug fix and 32.768KHz crystal oscillator stability issue. The PSRAM performance continues to remain the same though.

1. Hardware Design Changes:

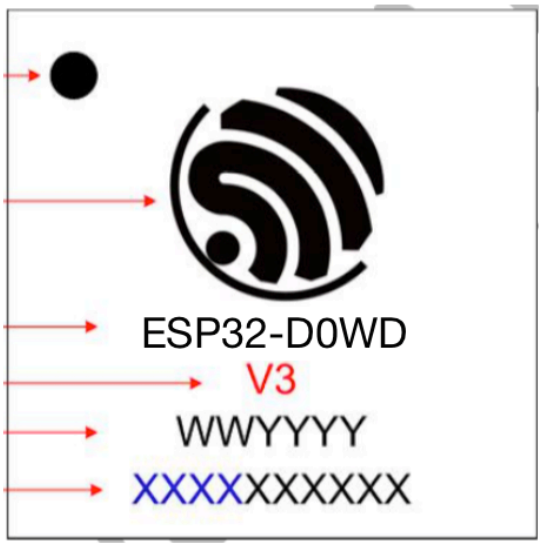
   Please follow latest *ESP32 Hardware Design Guidelines*.

2. Software Design Changes:

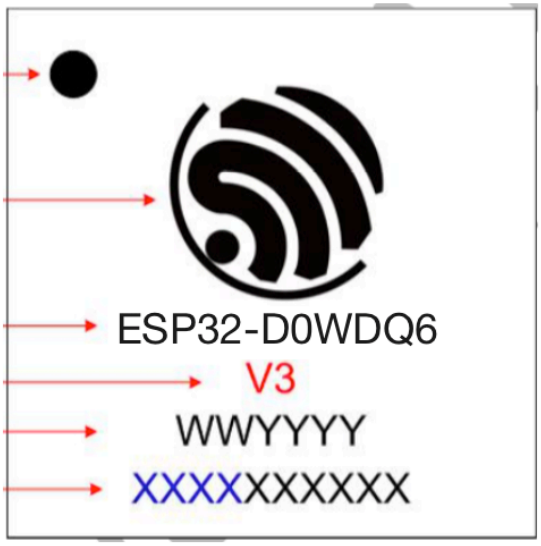
   Client can continue to use the same software and binary for deployed product. The same application binary will work on both chip revision v1.0 and chip revision v3.0.

3. Label Specification

The label of ESP32-D0WD-V3 is shown below:



The label of ESP32-D0WDQ6-V3 is shown below:



4. Ordering Information

For product ordering, please refer to: *ESP Product Selector*.

Espressif IoT Team

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